*WAVECREST Corporation*

# CHARACTERIZING JITTER ON RAMBUS® CLOCK SOURCES

Application Note No. 126

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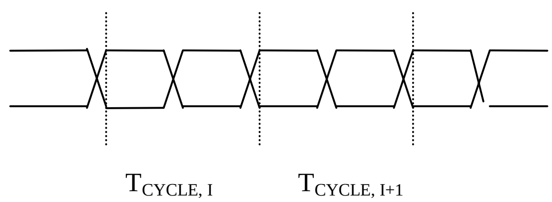
## INTRODUCTION

With the introduction of licensed Rambus® memory bus technology to volume semiconductor production, a new and challenging set of test and characterization issues are being confronted by engineers qualifying clock sources for a Rambus® memory system. The specifications of the Rambus® clock device require an operating frequency of 400MHz, 50ps of edge to edge jitter specification and a 4-cycle accumulated jitter spec of 100ps.[1] This application note will focus on techniques that the engineer can use when employing the *WAVECREST* DTS-2075™ and *Virtual Instruments*™ software tools to characterize, analyze and run production tests on Rambus® clock source chips.

### Rambus® Jitter Specification

The Rambus® Physical Layer Specification for Clock Sources[1] calls out two types of jitter. $T_{CYCLE}$ is the cycle-to-cycle jitter with respect to the falling edge of the CLK signal. The Rambus® specification defines this as the difference in cycle times of adjacent cycles. The second specification is called short-term jitter that is measured across adjacent 2-, 3- or 4-cycle periods. This application note will focus on measuring these specifications:

$T_J$ = Clock output cycle-to-cycle jitter = $T_{CYCLE,I} - T_{CYCLE,I+1}$




Other Specs:

$T_{J, IN}$ = RefClk input cycle to cycle jitter

$T_{J, short\ term}$ = short term jitter over 2,3,or 4 cycles.

$T_{4CYCLE}$ = 4 cycle jitter to 4 cycle jitter

Since the DTS makes one shot time measurements at random intervals, there is often a question as to how the instrument can correlate with a measurement of sequential cycles. This paper will demonstrate the statistics behind the cycle to cycle and short term jitter and how randomly sampling a waveform can provide exactly the same histograms and RMS jitter values and provide a more accurate measurement of the random events defined as “peaks”.

# SECTION 1 - APPLICATION SETUP and EXECUTION

## Equipment Setup

The following setup was used to create and measure a Rambus® system clock:

1) A *WAVECREST* DTS-2075™ measurement system and *Virtual Instruments*™ software. These instruments provide a measurement resolution of 800fs, a noise floor of 3ps and a measurement accuracy of +/- 10ps in burst mode.
2) A *WAVECREST* DTS-550™ Programmable data pattern generator. This instrument can provide a low noise clock waveform up to 1.06GHz with typically less than 10ps instrument jitter. This is a good lab source to generate a Rambus® system clock. The DTS-550™ can inject a known modulation frequency, amplitude and waveform into the clock output. This allows the application of controlled jitter modulation frequencies, step functions, and random jitter added with the capability of controlling the jitter magnitude unit interval. This generator can also provide a sync output that can be used to arm the DTS-2075™.

## Application Parameters

Three 400MHz clock waveforms with different jitter characteristics are used in this experiment. The first is a jitter modulation that contains a single deterministic sinusoidal modulation running at a 30kHz frequency with a 1.00ns peak jitter magnitude. This type of modulation causes the clock frequency to vary between 667MHz and 286MHz with the edge-to-edge changes varying at only a 30kHz rate.

The second modulation is a step function that jumps the period ±1ns at random intervals. This type of modulation simulates the intermittent, one-time events that are the most difficult for any instrument, whether a DTS, TIA, scope or digitizer, to capture (if enough samples or time is not allowed to capture the maximum random component).

The last experiment is performed on a low phase noise, 400MHz clock with no modulation. This will allow us to compare the modulation plots and measure the high frequency jitter most likely to affect a Rambus® clock system.

The following data is collected for each modulation setup.

1) Measure edge 1 to edge 2 jitter, and plot the histogram using the **Spectrum** Tool in *Virtual Instruments*™.
2) Measure the edge 1 to edge 3 jitter using the **Spectrum** Tool.
3) Measure the edge 1 to edge 4 jitter using the **Spectrum** Tool.
4) Repeat for edges 1 to 5, 1 to 6, 1 to 7 and 1 to 8.
5) Measure the Accumulated Jitter in the time domain for a complete modulation cycle.
6) Measure the Accumulated Jitter in the time domain for clock edges 1 to 4.
7) Measure the Accumulated Jitter in the time domain for clock edges 1 to 8.
8) Measure the Accumulated Jitter for a full modulation cycle.
9) Measure the Accumulated Peak Jitter across four clock edges.
10) Measure the Accumulated Peak Jitter across eight clock edges.

Once this data is collected, the effects of the different modulation types can be looked at in the frequency domain using the FFT capability of *Virtual Instruments*™ software.

## Source Data and Settings

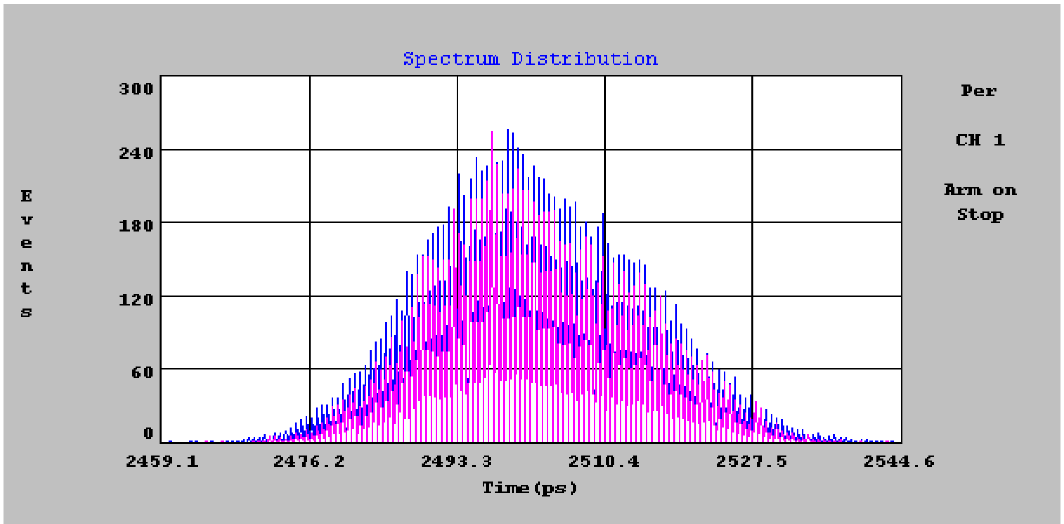
### 400MHz Clock, Sinusoidal Modulation
### *Virtual Instruments*™ - Spectrum Analysis window function (See manual for instructions.)

The first measurement taken was a histogram of the DTS-550™ clock output, running at 400MHz with a 30kHz, 1.0ns modulation. This type of modulation is typically found in clock sources using Spread Spectrum Clocking, but with much larger amplitude.

In *Virtual Instruments*™, the following measurement setup parameters in the **Function** pull-down menu were used:

**Function**................................ PER
**Channel** ................................ 1
**Start Volt**.............................. XXXX
**Stop Volt**............................... XXXX
**Sample Size** .......................... 10000
**Pulse Find %**........................ 50%-50%
**Arming**.................................. Arm on Stop
**Start Arming Event**............. 1
**Stop Arming Event**.............. 2

This setup results in 10,000 Period measurements being plotted. The period is measured from the first edge after the measurement enable of the second edge. Measurements are taken asynchronously at the 50% voltage point measured from the last executed Pulse Find operation. Finally, the Spectrum plot is taken using **Overlay**, so the results of all the measurements can be seen. Figure 1 is the histogram plot of these measurements.

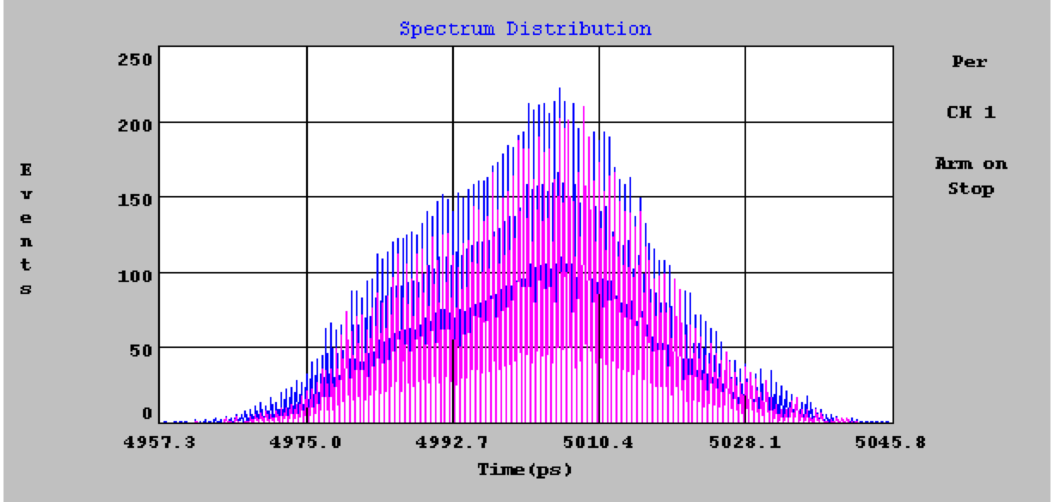



| | MEASURED | JITTER | Pk-Pk | MAXIMUM | MINIMUM | EVENTS | # PASSES |
|---|---|---|---|---|---|---|---|
| LATEST | 2502.0 | 11.5 | 78.7 | 2542.7 | 2464.0 | 10000 | |
| OVERALL | 2502.1 | 11.5 | 84.2 | 2543.9 | 2459.7 | 230000 | 23 |

**Figure 1 - Histogram of 30kHz Sinusoidal Modulation**

The DTS-2075™ measures 11.5ps of RMS jitter and worst case 84.2ps of peak-to-peak jitter. Where is the 30kHz modulation in this figure?

The plot in Figure 2 uses a **Stop Arming Event set** to 3. This means that the histogram will plot the time interval for edge 1 to edge 3. In the plot in Figure 1, the ***lowest*** frequency modulation that can be observed without loosing information is $Clock_{freq}/2$. Jitter at frequencies below $Clock_{freq}/2$ is rolled off at 20dB/decade. The lower cutoff frequency in Figure 2 is $Clock_{freq}/3$. Figure 2 shows what happens to the statistics for the signal when we look across 3 edges.




| | MEASURED | JITTER | Pk-Pk | MAXIMUM | MINIMUM | EVENTS | # PASSES |
|---|---|---|---|---|---|---|---|
| LATEST | 5002.7 | 13.1 | 80.0 | 5041.5 | 4961.5 | 10000 | |
| OVERALL | 5002.2 | 13.1 | 87.3 | 5045.2 | 4957.9 | 240000 | 24 |

**Figure 2 - Histogram for Edge 1 to Edge 3, or 3 Adjacent Clock Cycles**

Note how the RMS increased 1.6ps and the peak jitter increased about 3.1ps. The shape of the histogram also appears to invert with the asymmetry shifting toward the faster measurements. This indicates a high frequency modulation on the clock edges but we still see no effect from the 30kHz modulation. The histogram plots that follow will show how the jitter spectrum changes as the stop count increases.

Figure 3 is a histogram plot for edge 1 to edge 4. This setup covers the four sequential clock pulses called out for in the Rambus® clock spec. Note the RMS jitter increases or decreases as the cutoff frequency is lowered. We are seeing the effects of adjacent cycle jitter as we look at odd cycle combinations and even cycle results.

The peak to peak jitter is increasing. The larger capture window allows more noise from the 30kHz modulation to push into the measurement window, which raises the probability of a larger peak occurring. Also the amount of time we are measuring is increasing as the stop count increases. *Using the RMS value eliminates the random nature of the peak events and provides a more accurate measurement of the high frequency jitter effects in the clock source.* Peak values should really be characterized as *n* sigma numbers. A six-sigma maximum is common for this type of clock measurement.

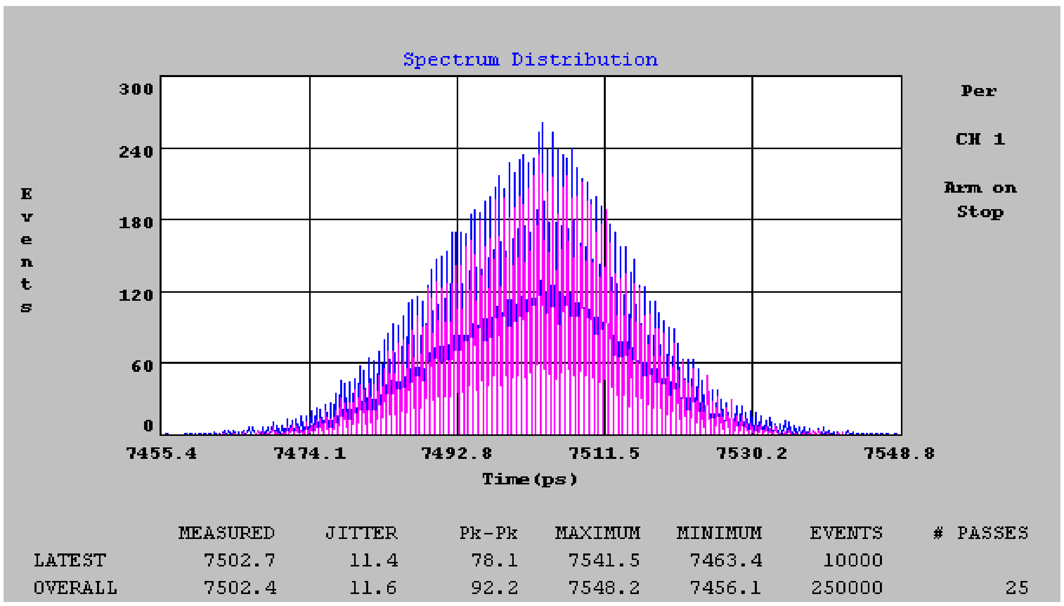



**Figure 3 - Histogram of Edge 1 to Edge 4 or 4 Adjacent Clock Edges**

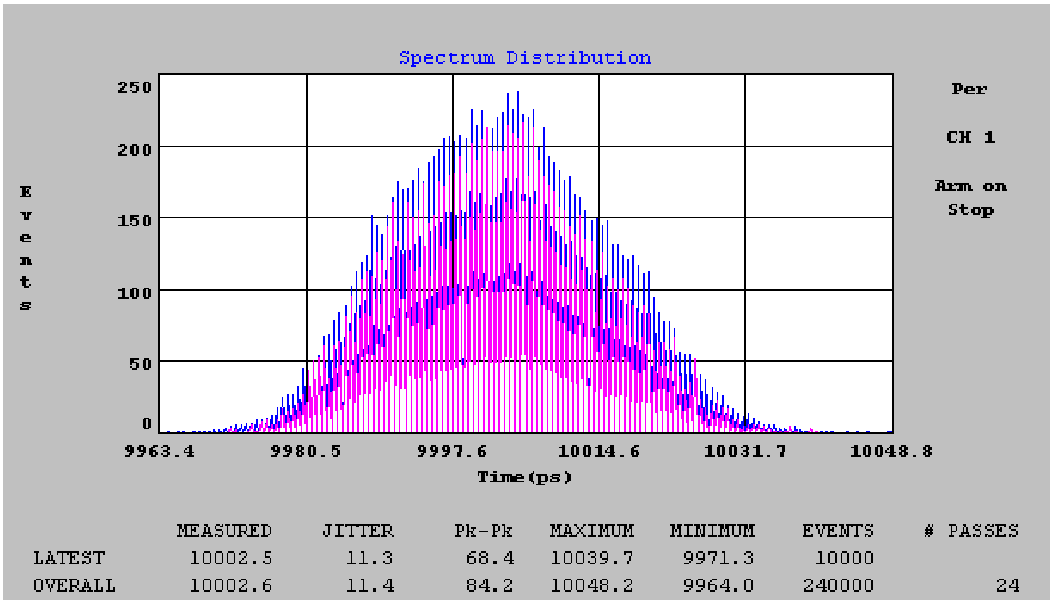



**Figure 4 - Histogram of edge 1 to edge 5**

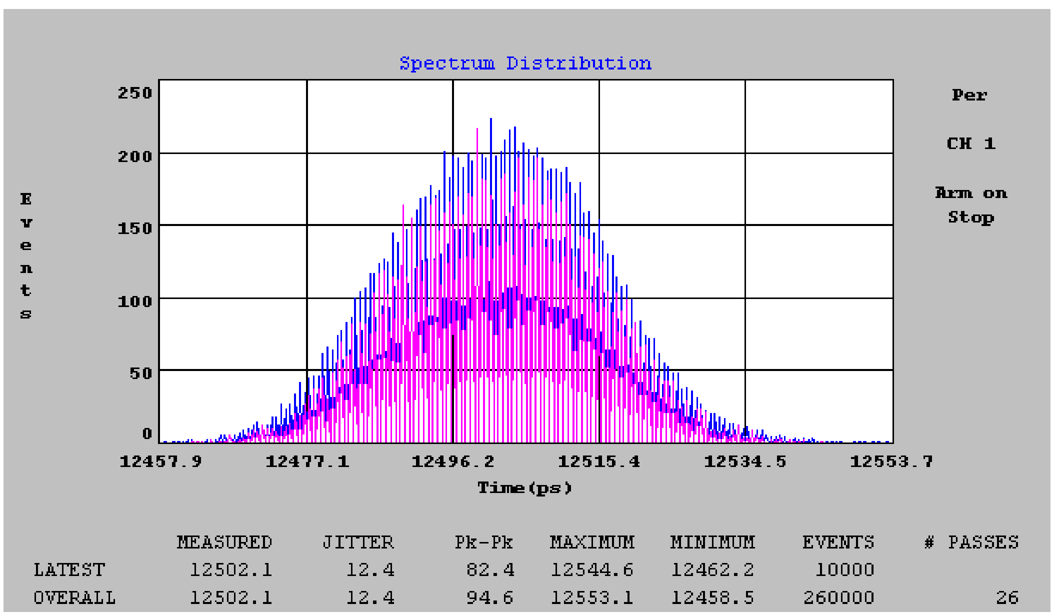



**Figure 5 - Histogram of 6 adjacent edges**

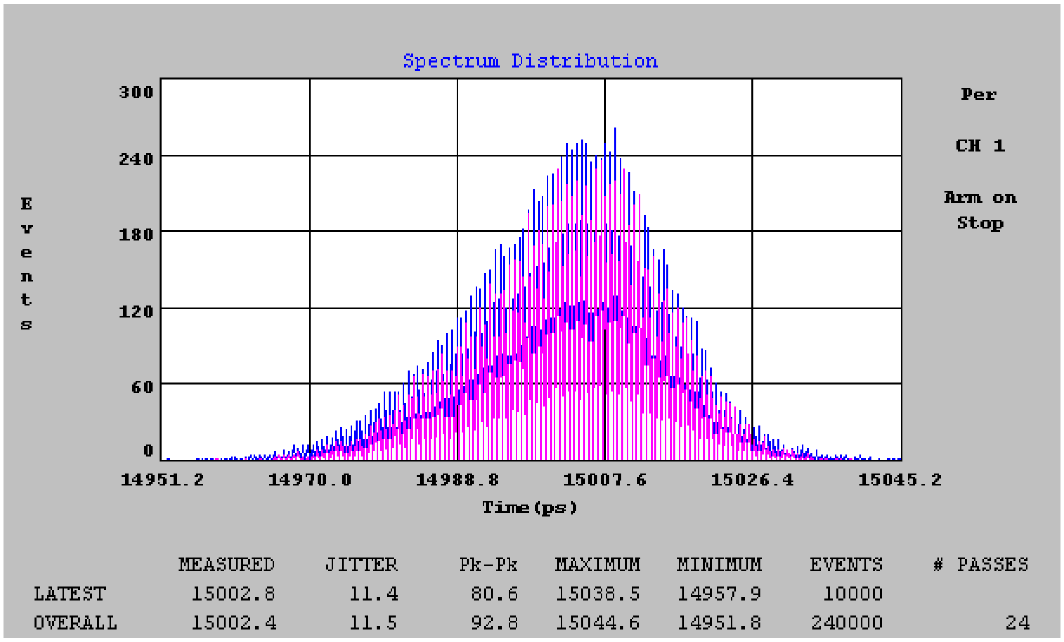



**Figure 6 - Histogram of 7 edges**

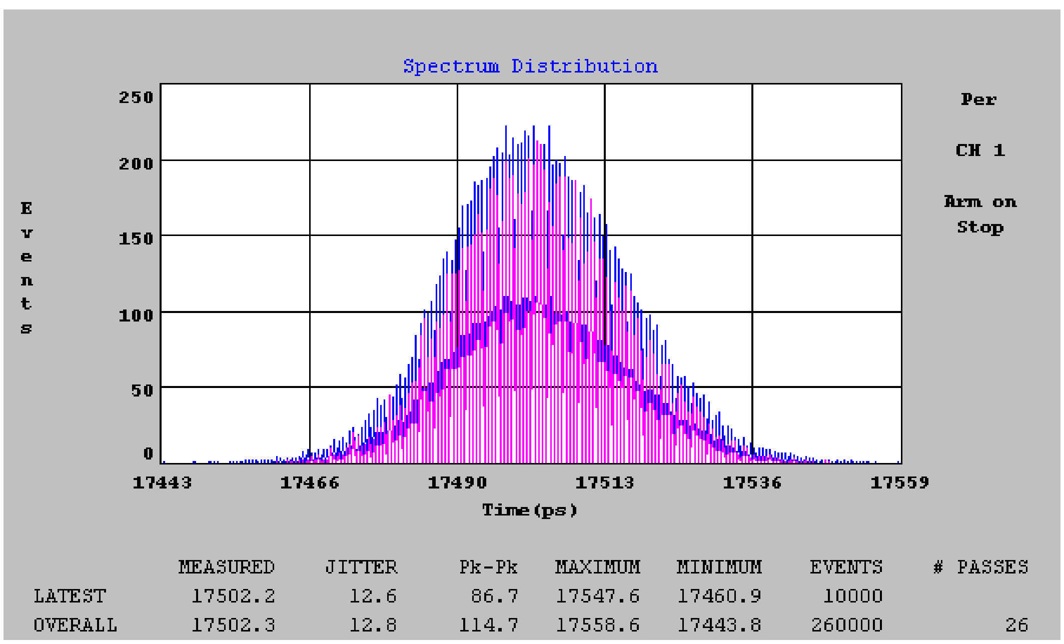



**Figure 7 - Histogram of 8 adjacent edges**

## Correlating Spectrum Results

These seven **Spectrum** plots are run in automatic mode. This method allows us to get a true look at worst case peak jitter for adjacent cycles. Since all single cycle measurements are displayed, and the measurements are taken randomly, the worst case *n* cycle measurement is displayed without any bias from the sequence that the clock events take place.

Since the issue with Rambus® clocks is to verify that the peak deviation on adjacent cycles are meeting spec, the DTS-2075™ measures random events and by definition, obtains the worst case adjacent cycles. If the clock is also measured with a digitizer, there are a number of correlation issues that needs to be resolved. First, in a sequential digitization, the display will only provide the actual worst case sequential events that occurred during the capture time. The results from a digitizer looking at adjacent cycles may closely approximate the RMS of the peak to peak values found on the DTS. The DTS-2075™ samples many more events over a much longer time span. Dividing the peak to peak value in the Spectrum plot by the square root of two can usually correlate results from a digitizer

Secondly, peak values measured on the DTS are random unbounded, random occurrences in the measurement population. As such, there is often instrument to instrument differences that must be accounted for. In the case of the DTS-2075™, a single measurement is subject to about 3ps of random noise floor and 10ps of absolute accuracy.

The **Jitter Analysis** tool described in the next section can provide us with more information and a better picture of the jitter relationship between adjacent edges than the **Spectrum** tool. Jitter Analysis provides plots of the jitter signature in both the time and frequency domains.

## Jitter Analysis, 30kHz Sinusoidal Modulation

The **Jitter Analysis** tool plots either the RMS or peak jitter as a function of clock event. This tool measures the jitter accumulation and modulation frequencies over a programmed range of stop events. The accumulated jitter can be displayed in either the time or frequency domain. These tools plot the RMS jitter versus the clock event, can pass the accumulated variance plot through an autocorrelation routine so that the engineer can take an FFT of the autocorrelation. This will measure the magnitude of deterministic frequency components of the jitter modulation and how these effect the 1 cycle, peak, *n*th cycle jitter and adjacent cycle jitter.

**Jitter Analysis** uses the Arm on Nth event counters to skip to the stop edge that defines the desired low frequency cutoff point. The algorithm the software uses to plot accumulated jitter for a period is:

1) A period measurement is made from start event one which is the first clock edge to the specified stop event which is initially set to 2 or the second clock edge. This is a period measurement and the measurement would have the same values as those in Figure 1.
2) The measurement is repeated for the specified sample size. In this experiment, the value was set to 1000. The start and stop edges are randomly selected.
3) The RMS jitter value is plotted referenced to the stop event.
4) The stop event is incremented by a user-specified value.
5) Steps 1-4 are repeated until the specified high stop count is reached.

Graphically, the measurement sequence is shown in Figure 8.

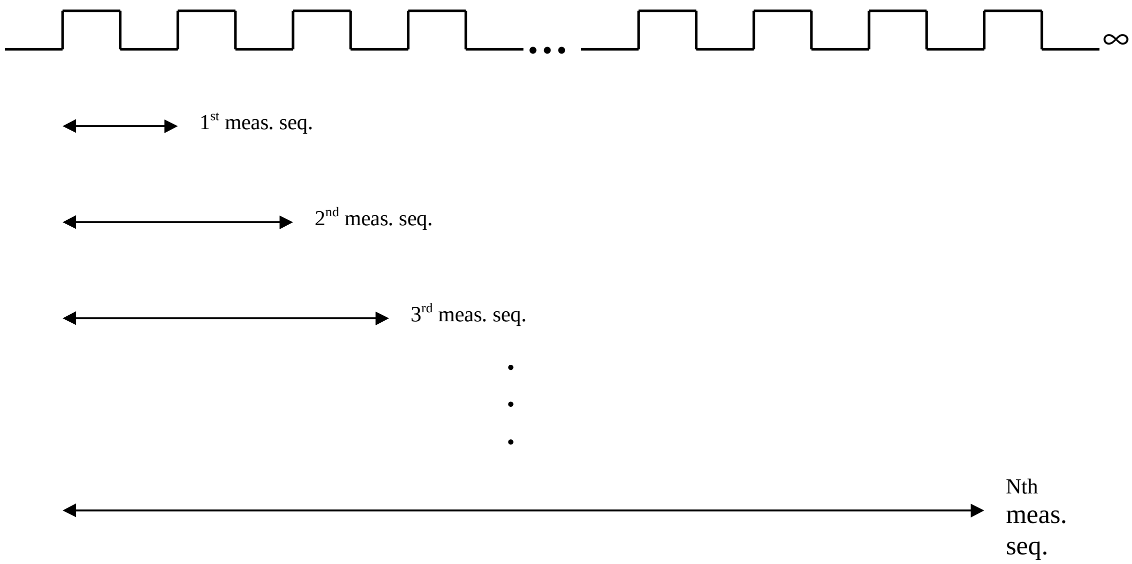



**Figure 8 - Jitter Analysis Algorithm**

The value N refers to the largest selected stop count. In the DTS-2075™ the maximum stop count the user can program is 131,072 ($2^{17}$). In order to observe a jitter modulation frequency, the user must program the high stop event counter to measure enough clock edges to capture a full cycle of the jitter modulation. The following equations define the parameters the engineer must use in the **Jitter Analysis** tool.

**Highest Observable Frequency:**

Clock Frequency/(Low Stop Count * Increment)
**Default:** Nyquist Rate or $Clock_{freq}/2$
**Note:** *Increasing the Increment reduces the Nyquist rate. By increasing the Increment, the engineer can provide more resolution at the lower end of the frequency spectrum.*

**Lowest Observable Frequency:**

Clock Frequency / High Stop Count
**Default:** None

In the case of the Rambus® 400MHz clock, the lowest frequency the **Jitter Analysis** tool can observe is 400MHz / 131,072 or 3052Hz. Also note that with an increment of 1, the highest observable jitter modulation frequency is Clock Freq. / 2 which is the Nyquist rate. Any jitter modulation at frequencies higher than the Nyquist rate will be seen as aliases at some frequency less than the Nyquist rate.

Figure 9 is a plot of a 30kHz jitter modulation, in the time domain. The y-axis is the accumulated RMS jitter. The x-axis is the clock edge defined by the stop count. The high stop count is set to 14,000 and the increment is set to 1. This gives a frequency range of 200MHz down to 28.751kHz.

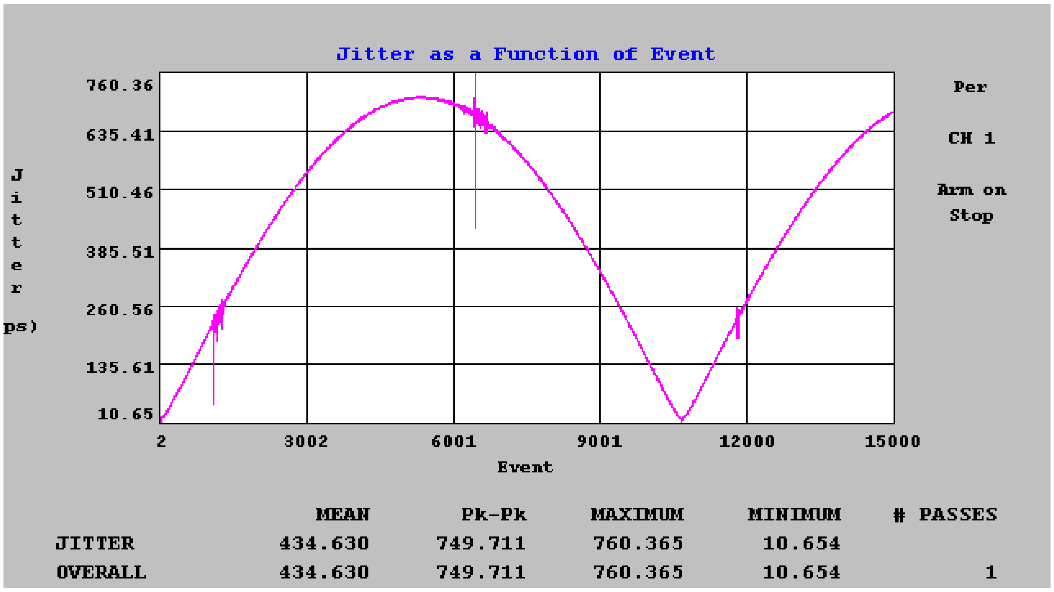
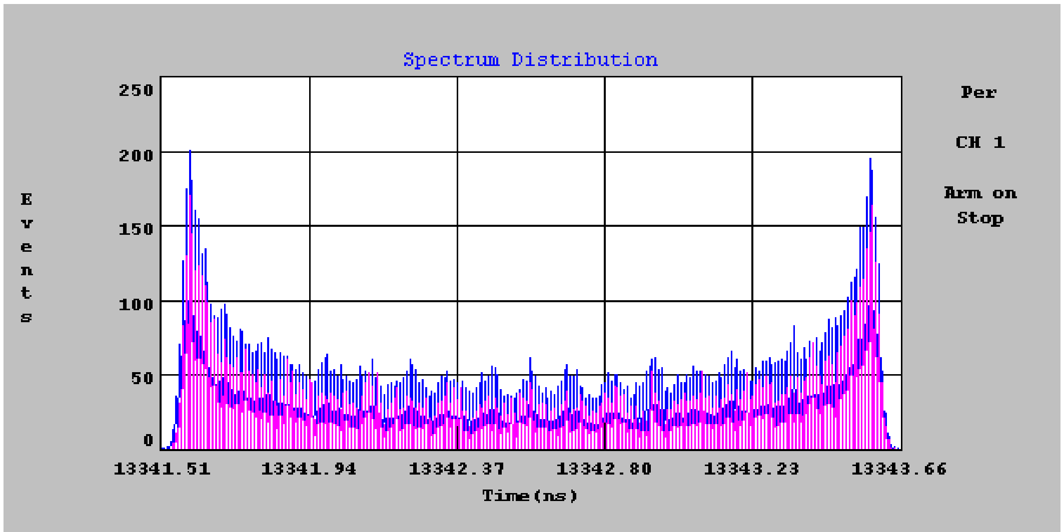



**Figure 9 - Accumulated Jitter with 30kHz, 1.00ns Sinusoidal Modulation**

In Figure 9, we see the full effects of the jitter. This graph *cannot be seen* in the **Spectrum** tool as it was set up, or any other measurement by the square root of two peak to peak method, such as an oscilloscope that observes less that the number of events needed to reach the modulation peak. Now we have the full picture of the jitter. The peak deviation is 744ps or RMS of the peak value. Note how the sinusoidal modulation causes the jitter to accumulate until the peak of the sinusoid is reached. Now, if we do a Spectrum measurement from 1 to edge 5344 (the modulation peak), the histogram correlates to the peak frequency modulation and the classic FM saddle associated with this type of modulation.

Figure 10 is a Spectrum plot of the jitter accumulation referenced from the zero crossing point to the peak of the sinusoidal jitter modulation function.




| | MEASURED | JITTER | Pk-Pk | MAXIMUM | MINIMUM | EVENTS | # PASSES |
|---|---|---|---|---|---|---|---|
| LATEST | 13342.6 | 0.707 | 2.1 | 13343.6 | 13341.5 | 10000 | |
| OVERALL | 13342.6 | 0.707 | 2.1 | 13343.6 | 13341.5 | 510000 | 51 |

**Figure 10 - Edge 1 to Edge 5366 Histogram**

Note the large peaks that correlate to the 2ns programmed peak-to-peak jitter from the DTS-550 ™ and a huge RMS measurement of 700ps. Remember though, this is a measurement from edge 1 to edge 5366. ***This is the setup in the DTS-2075 ™ that must be used to measure the peak period deviation produced by a low frequency modulation.*** The equivalent scope measurement setup would be to look at the jitter on the first edge and compare it to the jitter on the 5366$^{th}$ edge referenced to the first edge.

For a Rambus® device we only care about edge 1 to edge 4 and edges 1 to 8. This makes a big difference in RMS and peak measurements and lowers the measured jitter significantly. Why? *The Arm on Nth event counter is a high pass filter with the lower cutoff frequency set by the high stop count and the upper frequency set by the clock's Nyquist rate. Jitter below the frequency defined by (Clock-freq./High Stop Count) rolls off at 20dB/Decade.*

If we look at the jitter as a function of the Rambus® specification, we get the plot in Figure 11. This graph shows us the jitter accumulation across four adjacent clock edges. Now the numbers correlate with the spectrum plots in Figure 1 through 3. Note the small increase in the RMS jitter.

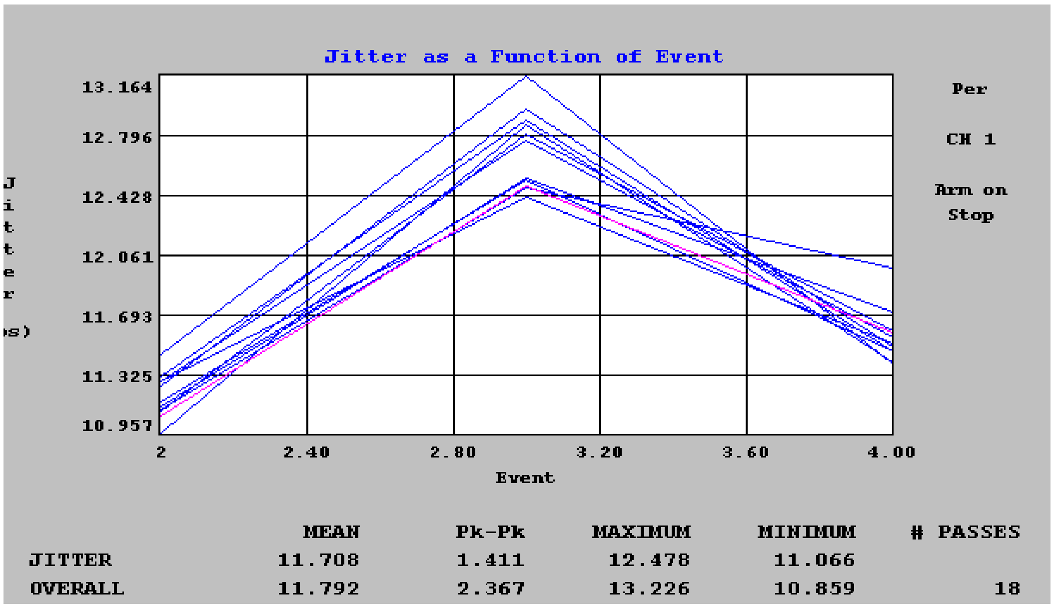



**Figure 11 - Accumulated Jitter with Respect to Four Adjacent Clock Edges**

If we plot the peak jitter for the four adjacent clock edges a similar correlation to the Spectrum plot can be seen. Figure 12 shows the peak values for the four consecutive clock edges.

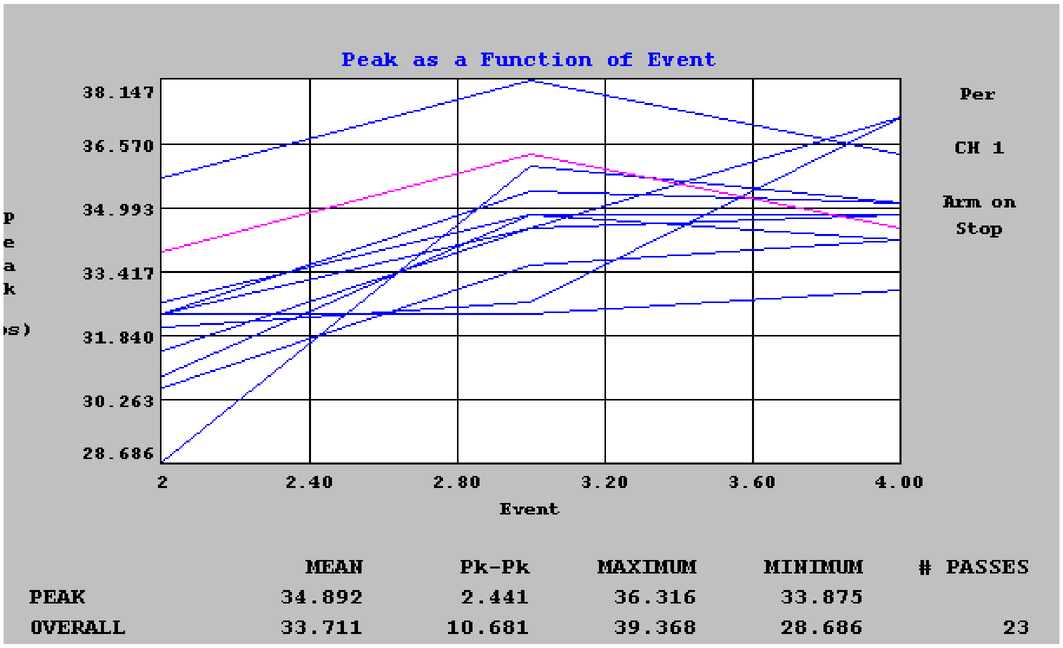
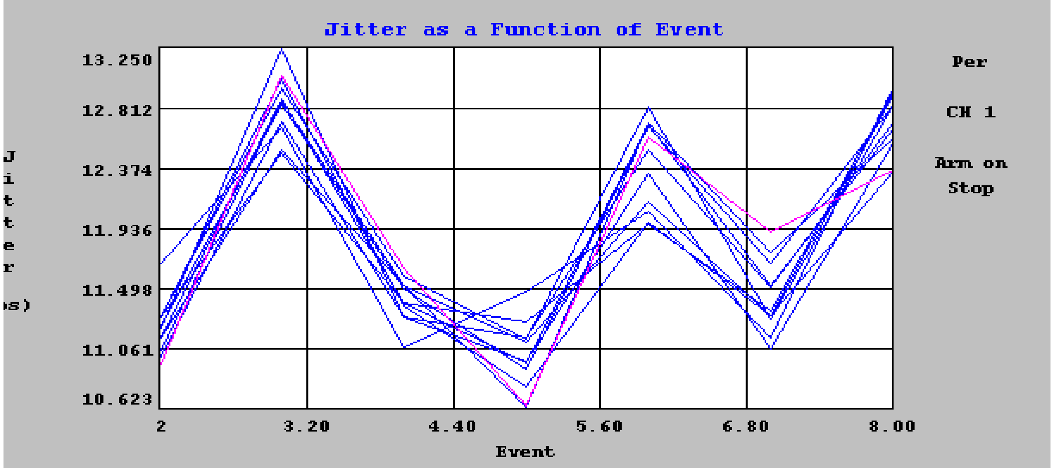



**Figure 12 - Accumulated Peak Jitter Across 4 Consecutive Clock Edges**

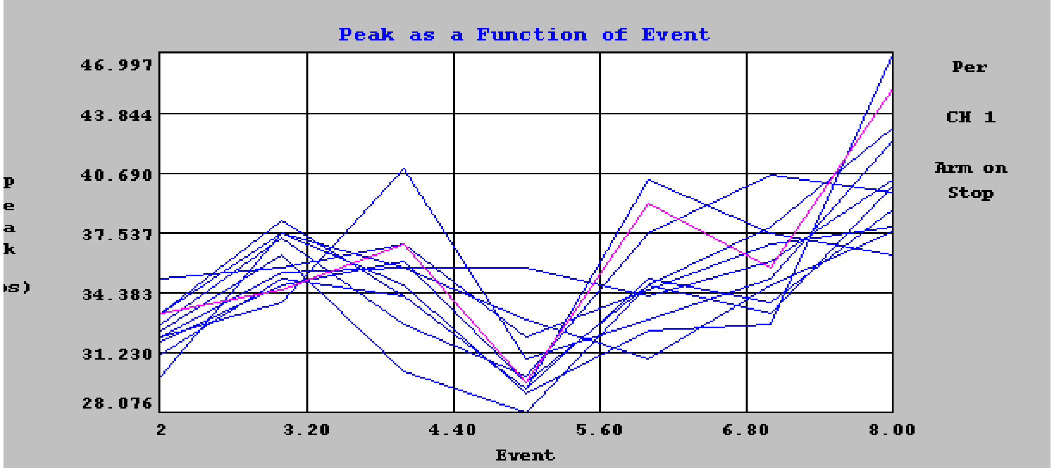
The peak jitter increases as the stop count increases. Doubling the values for peak in this graph gives good correlation to the peak to peak values seen in Figures 1 through 3. The one other thing to note is that since the peak events are essentially a function of random variability, there is much less coherency in the overlays.

Next we will take a measurement of the jitter as a function of eight cycles. Figure 13 shows the accumulated RMS jitter on 8 edges. Note the presence of the short long function and the good coherency from run to run. The peak, accumulated jitter is also shown in Figure 14. This is the measurement of the Rambus® $T_{4CYCLE}$ specification.




| | MEAN | Pk-Pk | MAXIMUM | MINIMUM | # PASSES |
|---|---|---|---|---|---|
| JITTER | 11.878 | 2.415 | 13.054 | 10.639 | |
| OVERALL | 11.864 | 2.771 | 13.250 | 10.479 | 22 |

**Figure 13 - RMS Jitter Across 8 Edges**




| | MEAN | Pk-Pk | MAXIMUM | MINIMUM | # PASSES |
|---|---|---|---|---|---|
| PEAK | 36.316 | 15.564 | 45.166 | 29.602 | |
| OVERALL | 35.283 | 20.141 | 48.217 | 28.076 | 20 |

**Figure 14 - Peak Jitter Across 8 Edges Rambus®**

Finally, the last point that will be explored in the 30kHz sinusoidal modulation experiment is an investigation of how the edge to edge measurements at the modulation peak correlates to the edge to edge measurements from edge 1 to edge 2. In this setup, we will set the start and stop counts for the measurement to 5338 and a stop count of 5339. Figure 15 shows the histogram.

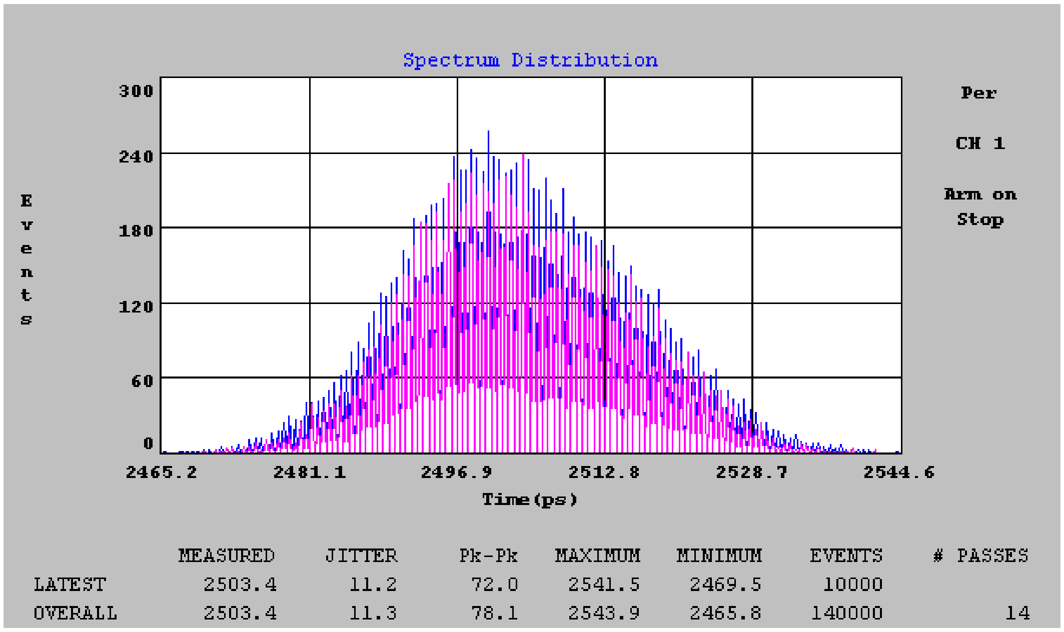



**Figure 15 - Jitter Measured at the Modulation Peak**

There is very good correlation between Figure 15 and Figure 1. This should be so since the random nature of the DTS-2075 ™ sampling will take measurements all along the modulation.

# SECTION 2 - STEP FUNCTION MODULATION

Since the DTS-2075™ employs a random sampling technique to acquire data, there is often a concern that intermittent, one period events will be missed by the instrument. This is a particularly important concern when testing synchronous systems where a dropped or drastically distorted single cycle is the worst case failure mechanism. Since the DTS-2075™ randomizes its sampling rate, if enough measurements are taken, any event which occurs periodically (the period could be hours) will be seen by the instrument. It is necessary to take enough measurement samples to provide a statistically valid set of data.

## Spectrum Tool Analysis of Step Function

As a means of demonstrating this, the DTS-550™ was programmed to provide a 1ns step discontinuity that ride atop the 30kHz sinusoidal modulation. The 30kHz spike will occur at the same point in the 30kHz waveform. The histogram for this modulation is shown in Figure 16.

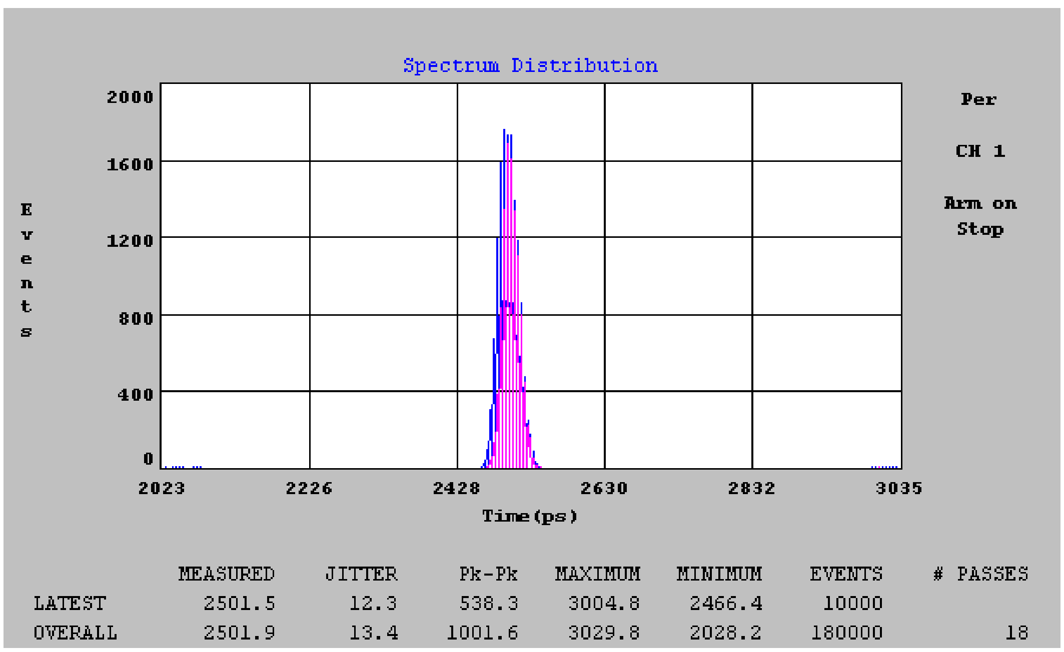
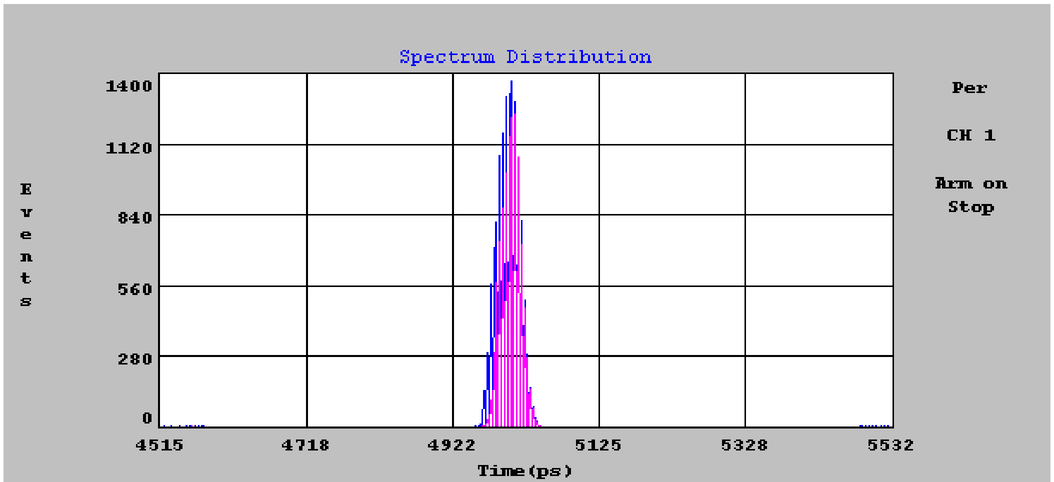



**Figure 16 - Histogram of Random Step Function Modulation**

This plot shows the single step functions modifying the period between 493MHz (2.028ns Minimum) and 330MHz (3.029ns maximum). This type of modulation would be a killer problem for a clock in a Rambus® application. In the case of sinusoidal modulation, each successive edge is modulated very slightly with respect to the last edge. In the step function modulation, any period can be followed by a very short or very long cycle.

By randomizing as the DTS-2075™ takes time measurements, we are assured to catch this discontinuity as long as we take enough samples. The frequency should be low enough for DTS sampling to catch it and if there are multiple frequencies to the step function, the DTS will still accurately measure the peak distortions. Note that with the sample size set to 10,000 the latest pass showed a peak value of 500ps, while the overall measurements see the true peak-to-peak value. Cycling the measurement insures that the proper distribution is measured.

Figure 17 is a plot of the edge 1 to edge 3 in the presence of the step modulation.




| | MEASURED | JITTER | Pk-Pk | MAXIMUM | MINIMUM | EVENTS | # PASSES |
|---|---|---|---|---|---|---|---|
| LATEST | 5001.9 | 13.7 | 483.4 | 5041.5 | 4558.1 | 10000 | |
| OVERALL | 5001.9 | 15.8 | 1008.3 | 5527.3 | 4519.0 | 130000 | 13 |

**Figure 17 - Edge1 to Edge 3 Jitter Spectrum for Step Modulation**

The RMS jitter stays about the same and the peak-to-peak values are similar. The RMS is a function of the large number of events in the center distribution while the peak events are now seen across 2 adjacent cycles showing us the worst case periods.

Figure 18 is the plot of clock edge 1 to clock edge 4 in the presence of the step modulation.

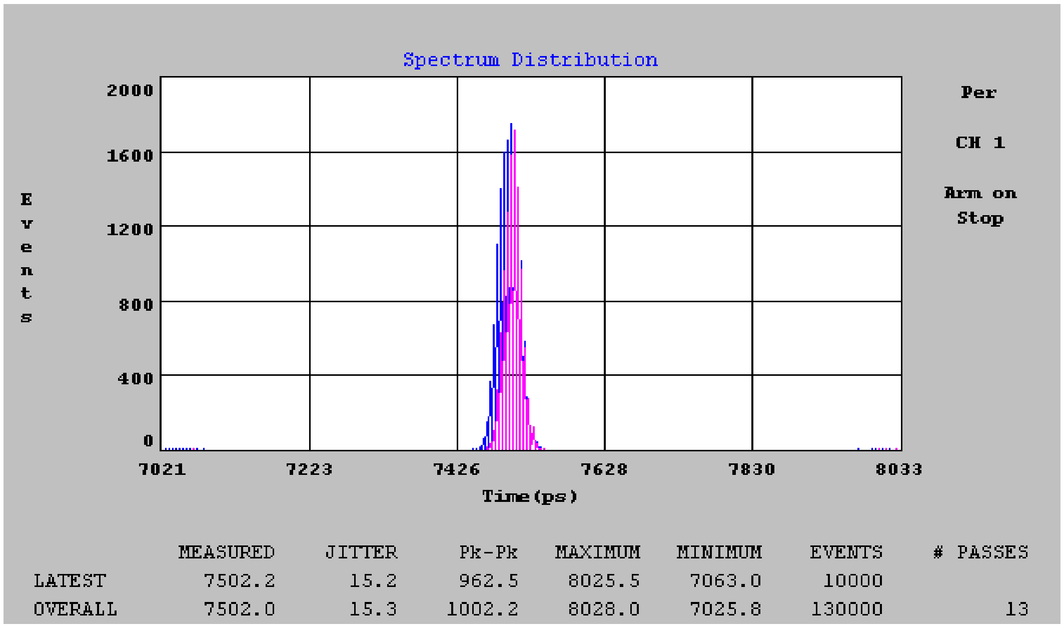
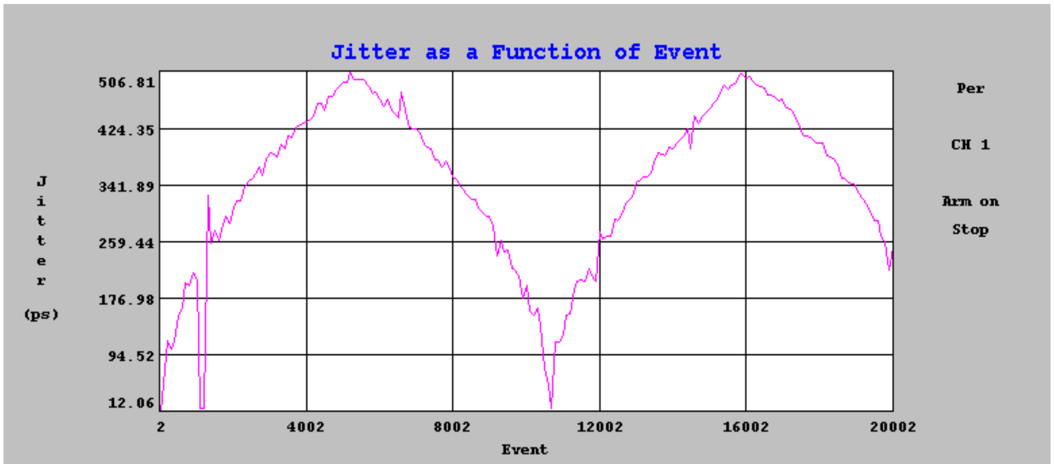



**Figure 18 - Edge 1 to Edge 4 Jitter Spectrum for Step Modulation**

## Accumulated Jitter Analysis of Step Modulation

The accumulated jitter plot of the step modulation displays some interesting traits. This plot was taken with the same setup conditions seen in the 30kHz sinusoidal modulation experiment.

Figure 19 shows the plot of the accumulated jitter for the step function. Note the shape of the jitter plot. The RMS jitter increases as the stop event is increased, the appearance of the random intervals changes the RMS accumulation numbers but the 30kHz sinusoid is still apparent. The shape of the accumulated modulation is more parabolic due to the noon-linearity of the random spikes programmed into the modulation.




| | MEAN | Pk-Pk | MAXIMUM | MINIMUM | # PASSES |
|---|---|---|---|---|---|
| JITTER | 344.165 | 494.742 | 506.806 | 12.064 | |
| OVERALL | 344.165 | 494.742 | 506.806 | 12.064 | 1 |

**Figure 19 - RMS Jitter Accumulation for 30kHz Step Function**

Of more interest is the Peak jitter accumulation across the full cycle of modulation. This plot should give us the maximum peak jitter envelope that this modulation source is creating. Figure 20 plots the peak jitter across 14,000 clock edges.

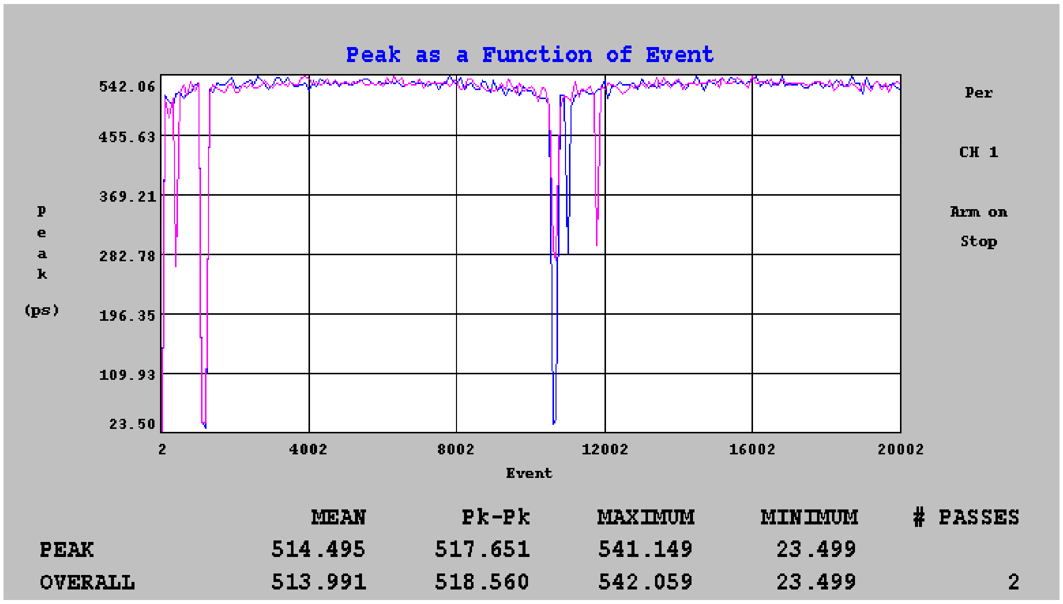



**Figure 20 - Accumulated Peak Jitter for Step Function Modulation**

This plot shows us the typical peak jitter at 500ps (1.0ns peak to peak) and the long-term worst case peaks. For a Rambus® clock we only need to measure 4 adjacent edges, however, the nature of this modulation means that we need to take a lot of samples to observe the random peaks, something that may or may not be possible with a digitizer.

For the Rambus® $T_{4CYCLE}$ specification, we measure the RMS jitter for 8 consecutive clock edges using 1000 samples at each point and obtain the plot in Figure 21.

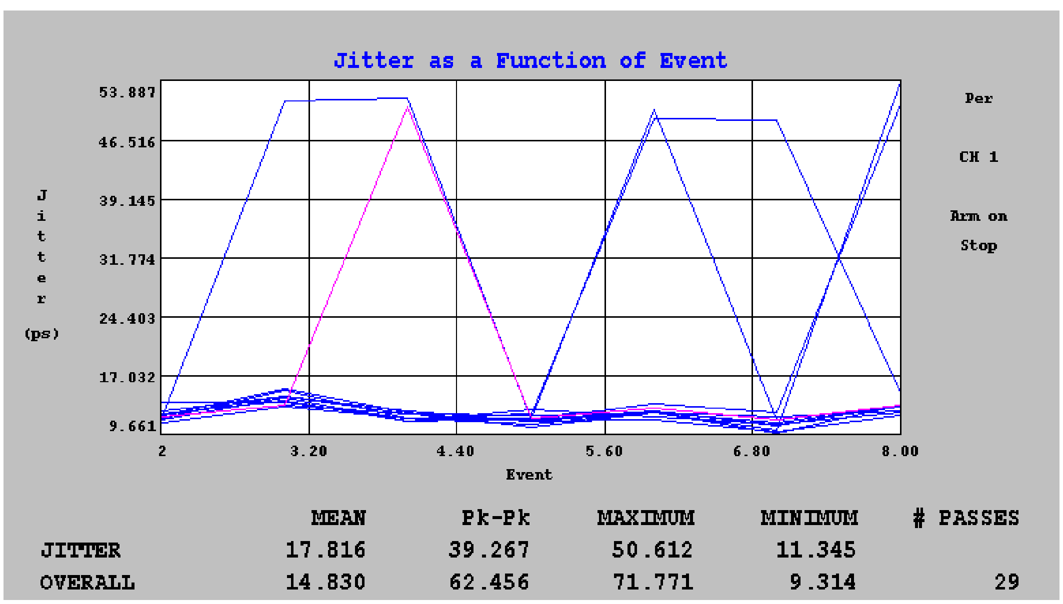
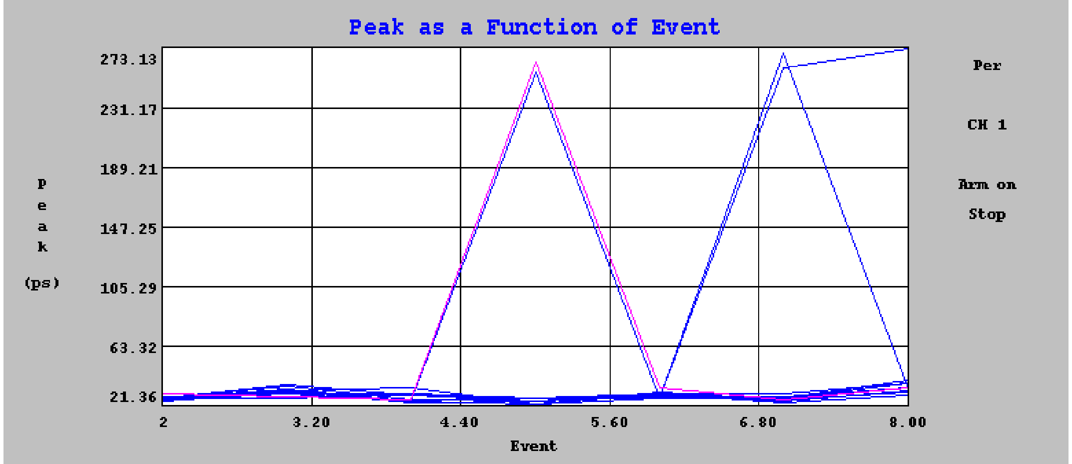



**Figure 21 - RMS Jitter for 4 Adjacent Clock Edges with Step Function Modulation**

This plot shows us a number of things about this clock source under this modulation. Most of the time the clock jitter is identical to the plots taken before. This is shown in the heavy lines at the bottom of the overlay plot that measure between 10 and 15ps RMS. The RMS jitter will occasionally jump up much higher. This indicates that there are multiple 500ps peaks in the measurement sample and that the probability of these events occurring on adjacent cycles is **not** zero. If it were the RMS, jitter would not vary as widely. Once again, the random sampling all along the modulation function is able to see the true statistical effects of the jitter.

Figure 22 shows the peak measurements for 8 adjacent edges. The peak events occur at random intervals and often are not seen in a single pass of the plot. This plot reports peak events, not peak to peak. In this case a 500ps peak to peak event is reported as 250ps or one half the peak to peak. Remember that there is a 1ns peak to peak event programmed on the source, the instrument will usually measure just one half of this peak in the sample time of the measurement, thus the reported peak of 250ps in the plot. What would be most interesting in this plot would be any deterministic frequencies of peak occurrences.




| | MEAN | Pk-Pk | MAXIMUM | MINIMUM | # PASSES |
|---|---|---|---|---|---|
| PEAK | 62.299 | 238.342 | 263.367 | 25.024 | |
| OVERALL | 44.613 | 260.010 | 280.456 | 20.447 | 55 |

**Figure 22 - Peak Accumulated Jitter Across 8 Adjacent Cycles**

# SECTION 3 - CLOCK ANALYSIS DATA WITH NO JITTER MODULATION

In order to give the data from the above two analysis sections some point of reference, the clock signal from the DTS-550™ with no applied modulation should be characterized. We are using this to look at high frequency modulations and this is most representative of the quality of a 400MHz clock source used for Rambus® applications

## Histogram Analysis Correlation

The histogram for the edge to edge measurement is shown in Figure 23.

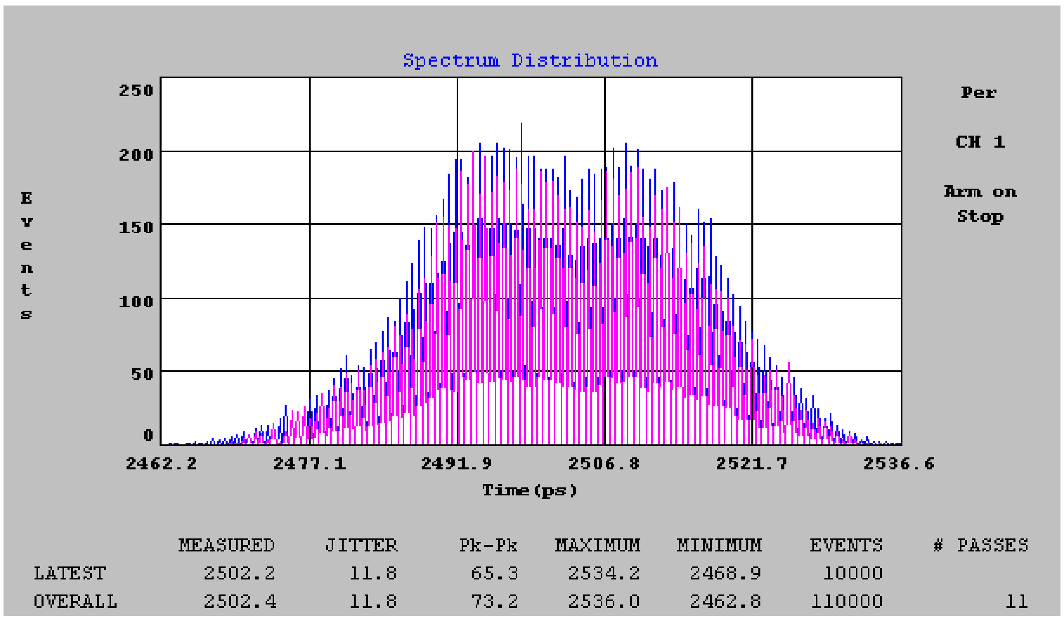



**Figure 23 - Histogram of 400 MHz Clock with No Modulation**

The RMS and peak jitters are very close to the plot in Figure 1. Note the shape of this histogram is bimodal indicating a high frequency modulation that was smoothed out in the presence of the 30kHz modulation. As we look out over multiple cycles this shape changes. In the case of adjacent cycles, Figure 24 is appropriate.

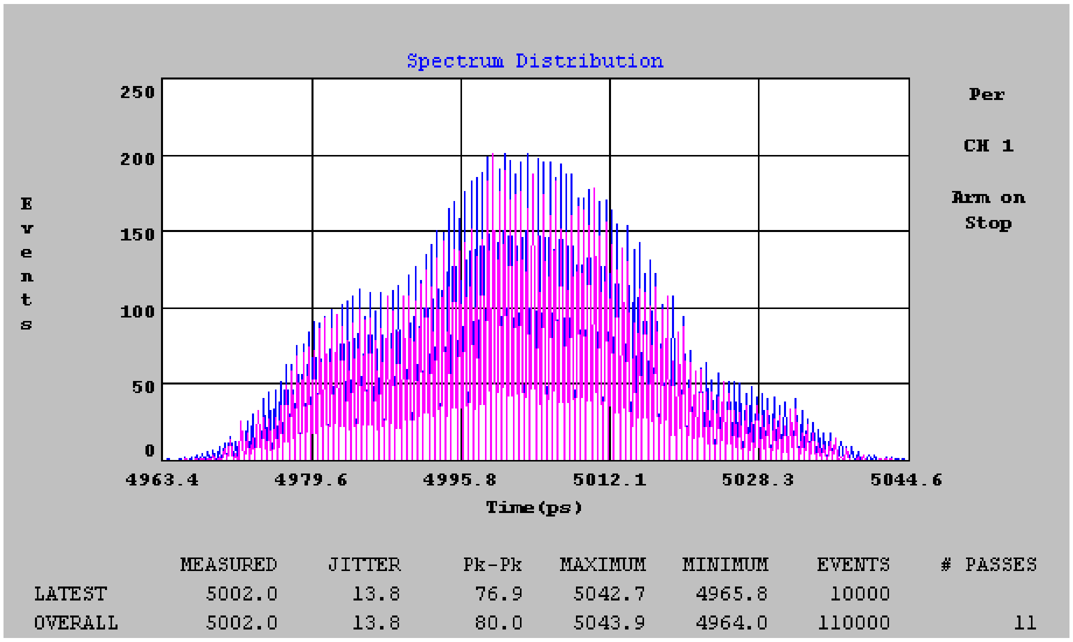



**Figure 24 - Histogram of Adjacent Edges with No Modulation**

Note the change in histogram shape as we bias our look at adjacent cycles, skipping every other edge.

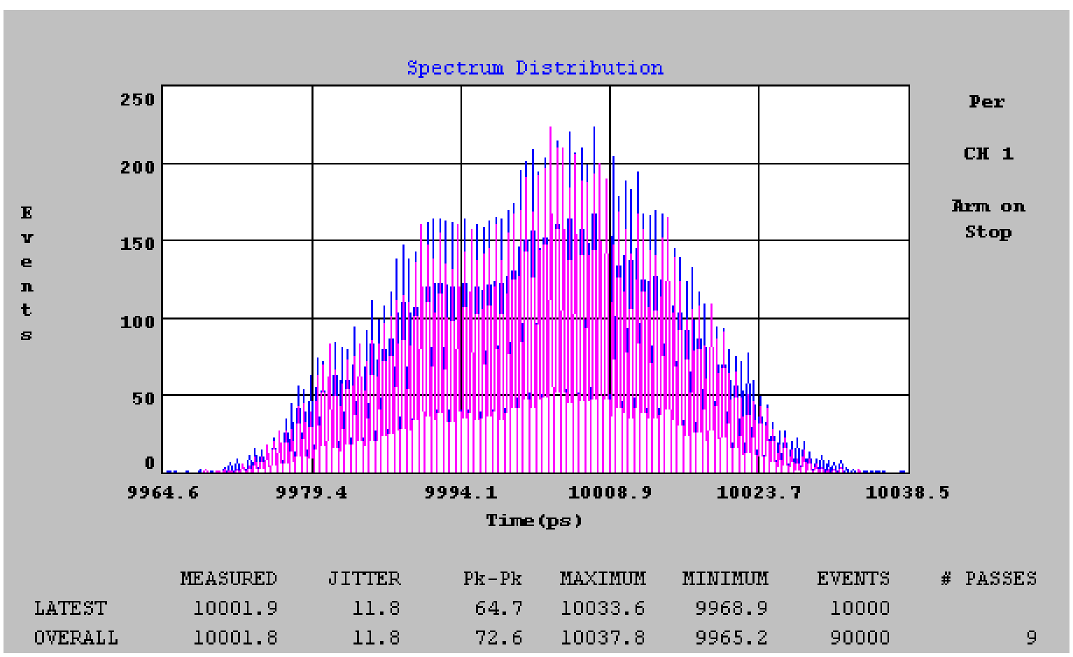
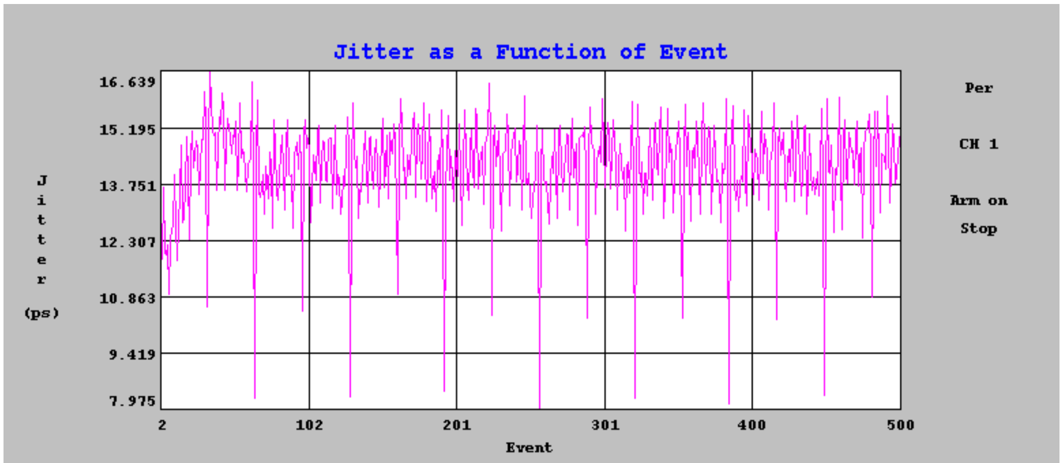



**Figure 25 - Histogram of 4 Adjacent Edges No Modulation**

## Jitter Analysis Correlation

The accumulated jitter of the 400MHz clock under a no modulation scenario is shown in Figure 26.




| | MEAN | Pk-Pk | MAXIMUM | MINIMUM | # PASSES |
|---|---|---|---|---|---|
| JITTER | 14.192 | 8.664 | 16.639 | 7.975 | |
| OVERALL | 14.192 | 8.664 | 16.639 | 7.975 | 1 |

**Figure 26 - Accumulated Jitter for 400 MHz Clock with No Modulation**

The interesting thing about Figure 25 is that we can observe the filter response of the DTS-550™ frequency synthesizer and would also be able to see the loop response of a PLL. At about 40 clock edges, the accumulated jitter has peaked, indicating a 10MHz cutoff frequency. The PLL stabilizes at a noise floor that has a mean of about 14ps and note that there is a feedback response that is modulating the jitter, indicated by the frequency of the null spikes above the settling point. This plot should be compared to the plots in Figure 9 and Figure 18. There is no low frequency modulation present in Figure 26.

If we want, we can take an FFT of this plot to extract those high frequency components that are modulating this signal. Figure 27 is an FFT plot of the autocorrelation of the variance seen in Figure 26.

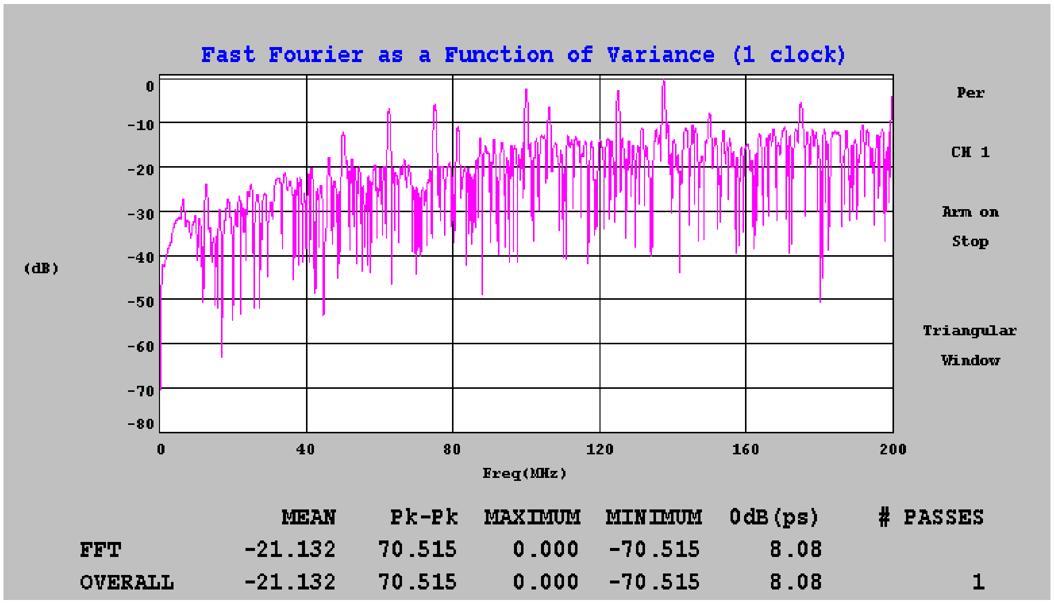
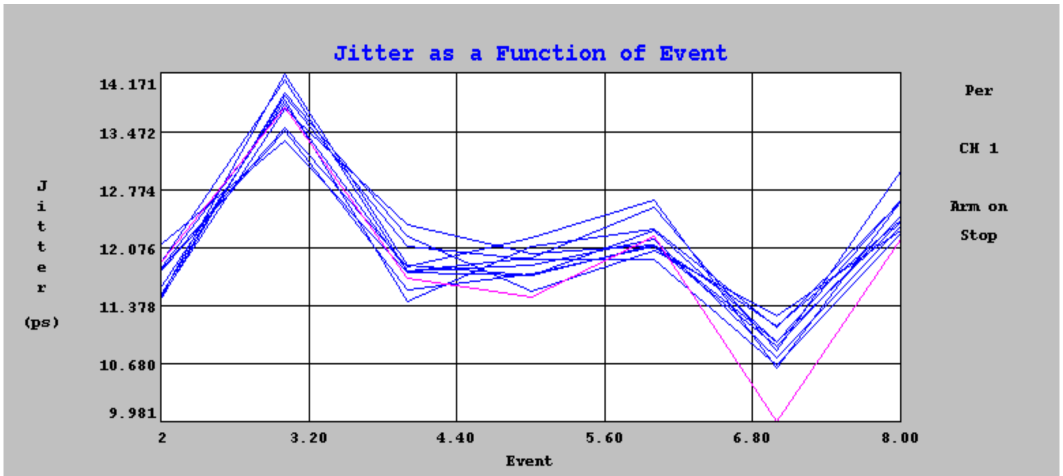



**Figure 27 - FFT Plot of Accumulated Jitter with No Modulation**

Note the Spectral lines that appear clearly at various frequencies. The highest spectral line is contributing 8ps of peak jitter (16ps peak to peak). This line occurs at the Nyquist frequency of 200MHz. There are also frequencies at 175MHz, 150MHz, 133MHz etc. These contribute less edge to edge jitter as they are farther from the Nyquist and have less effect on a single clock period.

## Rambus® 4 Cycle Analysis

The analysis of 8 adjacent edges in the no modulation environment presents a good look at the magnitude of the modulation function that we've seen as it applies to the Clock source. Since we see that there are high frequency modulations inherent on the clock from the FFT, we expect the accumulated jitter across 8 adjacent clock edges to show coherent effects of this modulation. This graph gives us the true statistical look at the jitter relationships on an edge to edge basis.




| | MEAN | Pk-Pk | MAXIMUM | MINIMUM | # PASSES |
|---|---|---|---|---|---|
| JITTER | 11.887 | 3.786 | 13.768 | 9.981 | |
| OVERALL | 12.110 | 4.189 | 14.171 | 9.981 | 13 |

**Figure 28 - Accumulated Jitter Over 8 Cycles, No Modulation**

# CONCLUSIONS

There are six conclusions we can draw from this experimental data. Each conclusion satisfies one of these two theorems from Digital Sampling and Communications Theory:

Theory 1: The **Highest** rate of information change or modulation is equal to the Carrier Frequency divided by 2. (Nyquist Rate)

Theory 2: The **Lowest** rate of change that can be observed in a modulated signal without loosing information is equal to the number of carrier edges that occur in the sample window. Information below the cutoff frequency defined by ($C_f$ / # edges captured) is lost at 20dB / decade.

These theorems apply to all instruments, oscilloscopes, TIAs, modulation domain analyzers BERT testers, spectrum analyzers and the DTS-2075™.

**Conclusion 1:** *Periodic jitter modulation at frequencies much lower than the Clock Carrier frequency has very little effect on the edge to edge jitter measurements. Digital Sampling theorem 2 is satisfied. We see this throughout the experiment where the sinusoidal 30kHz modulation is not observed in the Rambus® context.*

**Conclusion 2:** *Step functions at any frequency have a very large effect on both the RMS and Peak to Peak measurements. The ability of the instrument to observe random peaks is based on the instruments capture depth or ability to sample at random intervals. Sampling Theorem 2 is applicable to this conclusion. The data in Section 2 justifies this conclusion.*

If the engineer wants to calculate what the minimum sample size should be (in order to insure the probability that each clock cycle has been measured at least once and is very close to one), the following equation should be used:

Sample Size = Clock Freq. / Lowest Desired Measurement Freq.

For the 30 kHz step function:

Sample Size = 400 MHz / 30kHz =13,333

Doubling this value **guarantees** that the both the minimum and maximum step functions will be observed.

**Conclusion 3:** *To measure the peak RMS period deviation from a clock modulation, as referenced to the nominal period, a jitter accumulation measurement must be made across as many edges as necessary to span the lowest frequency modulation. Sampling Theorem 2 must be satisfied.*

**Conclusion 4:** *Random modulations and small scale deterministic modulations ride on top of the nominal low pass filter function of the PLL. Large-scale deterministic modulations swamp out the low pass filter curve.*

This conclusion is illustrated in the Jitter Analysis plots in Figures 9, 18 and 25. Observation of this data leads us to Conclusion 5, particularly if the histograms and accumulated jitter plots are reconciled properly.

**Conclusion 5:** *Jitter modulation at frequencies much lower than the Clock Carrier frequency have an extremely small effect on the accumulated jitter across 4 or 8 Rambus® clock edges. In order to satisfy Sampling theorem, any jitter modulation below (Clock $_{freq.}$ / High Stop Count) rolls off from this cutoff frequency at 20dB/Decade. See Conclusion 1 for edge to edge.*

From the data presented in Section 2, the following statement can be made:

**Conclusion 6:** *Peak Jitter is a" random" variable. This means that it is a single event and is theoretically unbounded and infinite. The number of samples collected by the measurement instrument defines its ability to capture a statistically valid peak event. As such, RMS jitter is usually the better method of measuring the true effects of jitter modulation in a circuit.*

Using the overlay method in the *Virtual Instruments*' Spectrum histogram and cycling through many measurements, one can observe the relationship between the overall population histogram and the latest pass histogram. If the latest pass is completely covered by the overall values, and the peak to peak value is no longer varying, there is a very high probability that the peak deviations have been captured for any reasonable measurement interval.

# SUMMARY

### Histogram Data

Table 1 below summarizes the data collected in this experiment for histogram data.

| | RMS Jitter | Peak Jitter |
|---|---|---|
| **No Modulation** | ***11.8ps*** | ***73.2ps*** |
| **30 kHz Sinusoid** | ***11.5ps*** | ***84.2ps*** |
| **30 kHz Step Function** | ***13.4ps*** | ***1001ps*** |

**Table 1**

### 4 Edge Accumulated Jitter

Table 2 summarizes the Rambus® specified 4 adjacent edge jitter accumulation.

| | Largest RMS Jitter | Peak Jitter |
|---|---|---|
| **No Modulation** | ***11.8ps*** | ***72.6ps*** |
| **30 kHz Sinusoid** | ***11.4ps*** | ***84.2ps*** |
| **30 kHz Step Function** | ***15.3ps*** | ***1002ps*** |

**Table 2**

These tables point out how small the effects are from adjacent edges to 4 edges. Low frequency jitter modulation has no measurable effect on the adjacent high frequency clocks. The summary table also graphically points out how difficult it is to use a clock that has a step discontinuity while a smoothly modulating jitter function, even when it has a very large UI magnitude, can still meet a synchronous system's performance parameters. These are exactly the parameters we see specified in the $T_{4cycle}$ and $T_{CYCLE}$ Rambus® spec.

### References


1: Direct Rambus® Clock Generator Specification, Version 0.8
pg. 4-10 - 4-12, pg. 6-5, Rambus Corporation



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