WAVECREST

Be certain of the signal you send.

SIA Family

Signal Integrity Analysis Solutions

specifications & options

SIA Family

The transition to multi-Gigabit serial data links introduces significant signal integrity design and system challenges. At these high data rates, signal integrity becomes the most critical test for determining overall performance and interoperability. Wavecrest instruments have offered high-speed test capabilities to design engineers for over 10 years. This experience enables us to provide you with all the compliance and diagnostic tools for most Datacom applications including:

- Fibre Channel
- Gigabit Ethernet
- SATA
- PCI Express™
- Infiniband

The Wavecrest SIA Family of Signal Integrity Analysis Solutions provides both timing and amplitude compliance measurements in any environment, system or IC, electrical or optical. Clock signals up to 6GHz and Data up to 4.5Gb/s* can be analyzed. Compliance tests can be completed in seconds with a simple pass/fail indication for each test parameter.

These solutions are the most comprehensive compliance and diagnostic signal integrity test solutions on the market today. The SIA "D" models come complete with the software necessary for Datacom analysis as well as powerful software for characterizing Clocks and PLL outputs. The SIA "C" models come complete with Clock and PLL analysis software.

SIA Model	Application	Clock Signal Timing Measurement Frequency	Data Signal Timing Measurement Frequency	Oscilloscope Bandwidth	Number of Channels**	Pattern Marker Option	Clock Recovery Option
3600D	Datacom	6 GHz	4.5* Gb/s	6 GHz	2, 4 or 5	Up to 5 Gb/s	30 Mb/s to 3 Gb/s
3300D	Datacom	Up to 2.5 GHz	Up to 2.5 Gb/s	6 GHz	2, 4 or 5	Up to 5 Gb/s	30 Mb/s to 3 Gb/s
3100D	Datacom	Up to 1.3 GHz	Up to 1.3 Gb/s	6 GHz	2, 4 or 5	—	—
3600C	Clock	6 GHz	—	6 GHz	2, 5 or 10	—	—
3300C	Clock	2.5 GHz	—	6 GHz	2, 5 or 10	—	—
3100C	Clock	1.3 GHz	—	6 GHz	2, 5 or 10	—	—

* Full RJ, DJ, PJ, DCD+ISI analysis to 4.5 Gb/s Data. Partial analysis beyond 6 Gb/s Data

** Custom number of channels available

specifications & options

SIA Family
Measurement Performance Specifications

TIMING

Clock Jitter

Applicable Models: **3600D, 3300D, 3100D**
3600C, 3300C, 3100C

The stable time base of the SIA Family provides the ability to perform time interval measurements over a broad time span without a significant increase in the wideband jitter noise floor. The frequency range for jitter measurements is 0.4 Hz - 1.3/2.5/6 GHz.

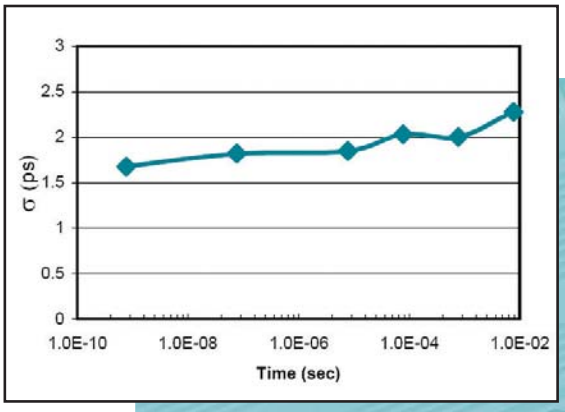
Data in Plot 1 was acquired with a 1.3 GHz, sine wave. Plot 1 shows the δ (standard deviation) of a histogram with 10,000 hits for time intervals ranging from 769 ps (1 period) to 7.69 ms (10,000,000) periods. The guaranteed noise floor specification, is < 3 ps rms (2 ps typical) for a 1,000 sample period measurement with 1.0 Vpp, 0.500-6 GHz sine wave input.

Plot 2 shows the typical rms jitter versus slew rate. The plot shows that to maintain a RJ noise floor below 3 ps rms the slew rate must be >0.5 V/ns.

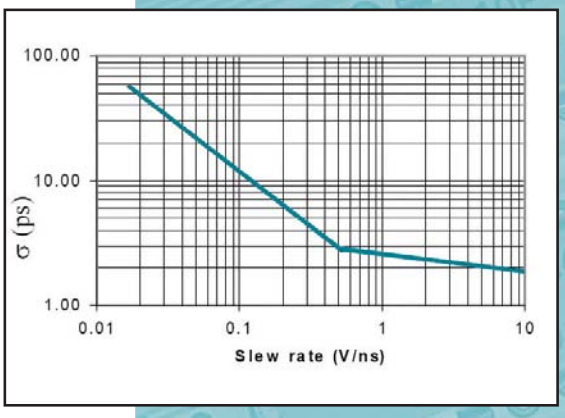
Plot 3 illustrates the capability of the clock analysis tools to isolate periodic components and quantify jitter over a user-defined bandwidth. The plot shows a spectral view of jitter measured from 12 kHz to 613 MHz of a 2.5 GHz sine wave. A 70 MHz sine wave was added to the carrier having a magnitude of 10 ps. Post processing filters provide the ability to determine the rms noise over a bandwidth. For example, the typical rms jitter from 12 kHz to 20 MHz is 400 fs determined from this plot.

The Low Frequency Modulation tool provides the capability of measuring low frequency (<100 kHz) periodic components on a carrier. Plot 4 shows the spectral view of jitter over 1 clock period from 0 Hz to 10 kHz of a 1.3 GHz sinewave modulated with a 50 Hz peak deviation 1 kHz sinewave. The 1 kHz spectral component has a magnitude of 31 as and the background noise is <1 as.

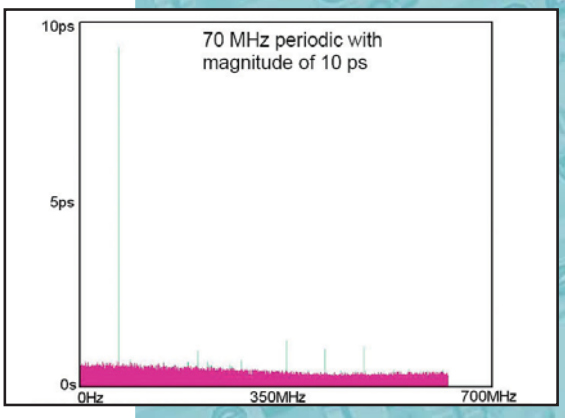
NOTE: 1 attosecond (as) equals 10^{-18}



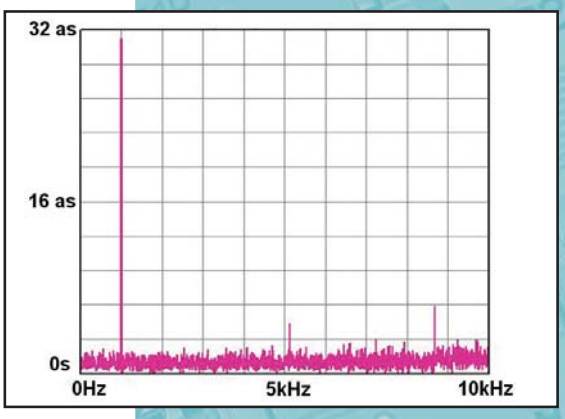
Plot 1



Plot 2



Plot 3



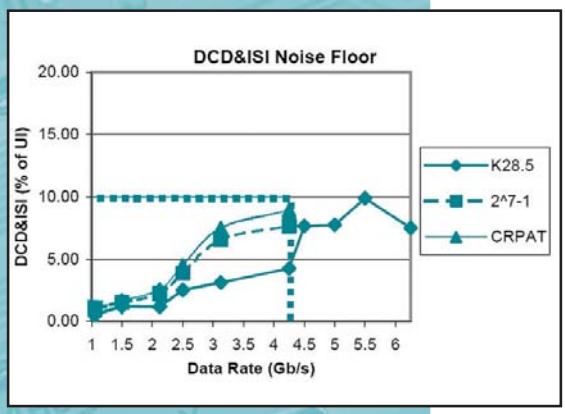
Plot 4

Data Jitter

Applicable Model: 3600D

Data Rate Range	up to 4.5 Gb/s
DCD&ISI	< 10% UI using CRPAT as the test pattern
RJ	800 fs typical across the bandwidth from the Nyquist of the bitrate to bitrate/1667

Plot 5 shows typical instrumentation DCD&ISI performance at various data rates and data patterns. The dashed line represents the guaranteed DCD&ISI specification limit tested at 1.0625, 1.5, 2.125, 2.5, 3.125 and 4.25 Gb/s. Noise floor measurements include the contributions from the pattern generator and cables. Plot 5 shows the typical DCD&ISI noise floor remains below 10% UI up to 6.25 Gb/s for K28.5.

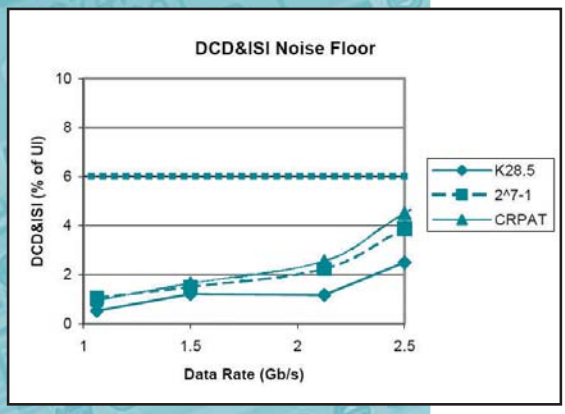


Plot 5

Applicable Model: 3300D

Data Rate Range	up to 2.5 Gb/s
DCD&ISI	< 6% UI using CRPAT as the test pattern
RJ	800 fs typical across the bandwidth from the Nyquist of the bitrate to bitrate/1667

Plot 6 shows typical instrumentation DCD&ISI performance at various data rates and data patterns. The dashed line represents the guaranteed DCD&ISI specification limit tested at 1.0625, 1.5, 2.125, 2.5Gb/s. DCD&ISI measurements include the contributions from the pattern generator and cables.

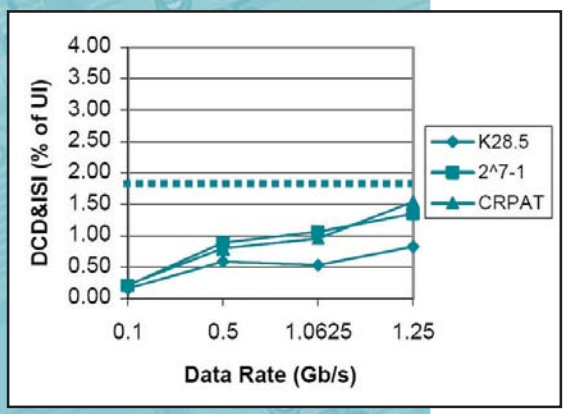


Plot 6

Applicable Model: 3100D

Data Rate Range	up to 1.3 Gb/s
DCD&ISI	< 3% UI using CRPAT as the test pattern
RJ	800 fs typical across the bandwidth from the Nyquist of the bitrate to bitrate/1667

Plot 7 shows typical instrumentation DCD&ISI performance at various data rates and data patterns. The dashed line represents the guaranteed DCD&ISI specification limit tested at 1.0625, and 1.25Gb/s. DCD&ISI measurements include the contributions from the pattern generator and cables.

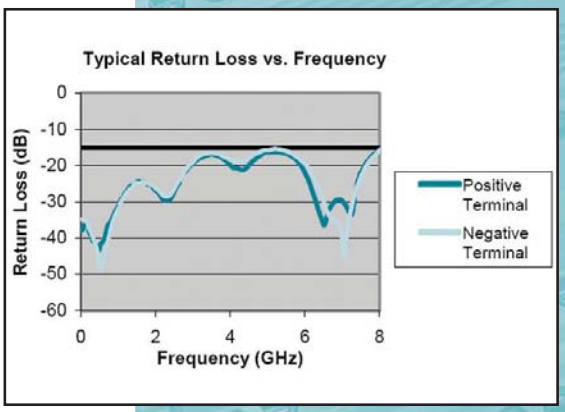


Plot 7

Internal Timing Reference

Applicable Models: 3600D, 3300D, 3100D
3600C, 3300C, 3100C

Frequency	10 MHz
Aging/year (after 24 hrs on)	1.5×10^{-7}
Aging/day (after 24 hrs on)	1×10^{-9}
Short term (1 sec) stability	5×10^{-11} (after 1 hr on)



Plot 8

Voltage Performance

Applicable Models: 3600D, 3300D, 3100D
3600C, 3300C, 3100C

Input voltage range ±1.5 V

The Input Voltage Range is defined as the minimum and maximum input voltage levels, relative to chassis ground, that the inputs can safely accept and meet performance specifications.

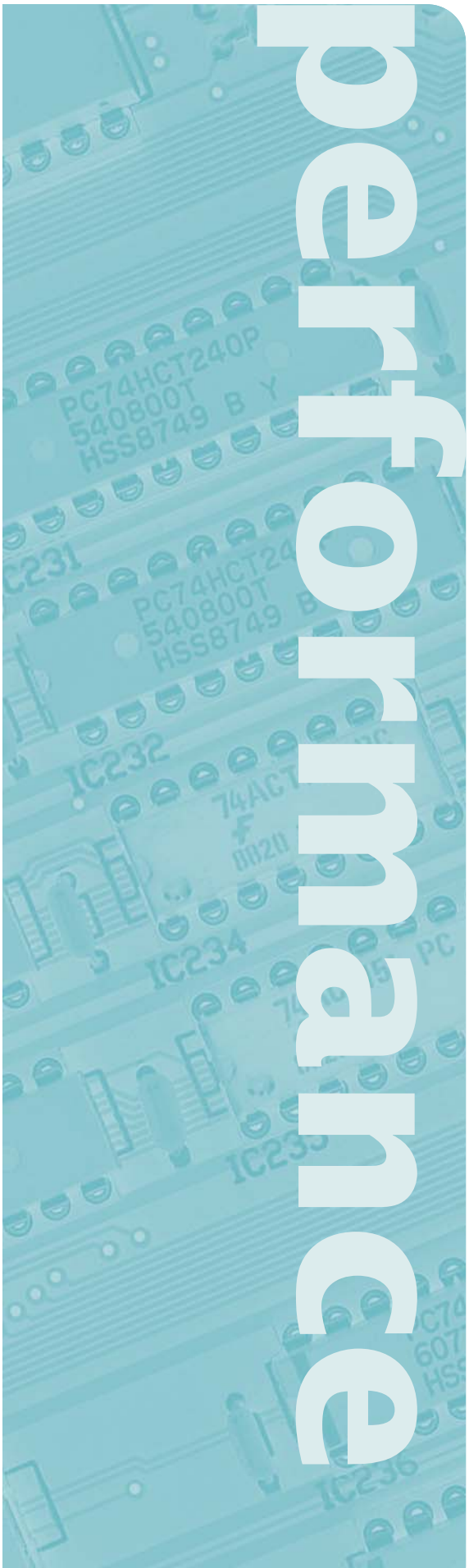
Electrical Input	Female SMA
Input Sensitivity	50 mVpp differential 100 mVpp single-ended
Return Loss	With respect to 50 less than -15 dB from 10 MHz to 6 GHz as shown in Plot 8.

Standard Timing Measurements and Features

Applicable Models: 3600D, 3300D, 3100D
3600C, 3300C, 3100C

Random Jitter, Deterministic Jitter, DCD&ISI, BER, Periodic Jitter, Skew, Propagation Delay, Period Jitter, Pulse Width Jitter, Cycle-to-Cycle Jitter, RMS Jitter over a bandwidth, Duty Cycle, Frequency, Damping Factor, Natural Frequency, Lock Range, Lock-in Time, Pull-in Time, Pull-out Range, Noise Bandwidth, PSD of Noise, Poles and Zeros.

amplitude



AMPLITUDE PERFORMANCE

Applicable Models: 3600D, 3300D, 3100D
3600C, 3300C, 3100C

Analog Bandwidth (-3 dB)	>6 GHz
Rise Time	60 ps (10% to 90%, calculated from RT=0.35/BW)
DC Voltage Accuracy	+/-(5mV + 0.5% _ offset voltage)
Input Dynamic Range	1 Vpp (Single-ended)
RMS Noise	<4 mV

Horizontal System

Delay	
Minimum	>24ns
Maximum	100 µs
Oscilloscope timebase jitter (rms)*	<1 ps + 10 ppm of delay setting
*Any additional trigger error will increase this value	
Timebase Delay Accuracy	<8 ps + 0.1% of delay
Time Interval Resolution	300 fs

Vertical System

Vertical Resolution	300 µV

Trigger Modes

Self Trigger (for clock patterns only up to 6 GHz)
External Trigger (up to 6 GHz)
Internal Pattern Trigger Options: Directly connected from PM50 or Clock Recovery

Standard Amplitude Measurements and Features

Rise Time, Fall Time, Overshoot, Undershoot, V_{max}, V_{mid}, V_{min}, V_{top}, V_{base}, $V_{pk\text{-}pk}$, V_{amp}, V_{RMS}, V_{AVG}, Mask Violations, Mask Comparisons, Horizontal and Vertical histograms and statistics.

Note: Typical measurements provide non-warranted information about system performance or capabilities.

OPTIONS

options

PM50
Pattern Marker and Bit Error Counter

Applicable Models: 3600D, 3300D

Traditionally, performing jitter measurements on systems has been difficult because it required the use of a bit clock or trigger, which has typically been unavailable. The Pattern Marker option for the SIA 3600D and 3300D enables jitter compliance measurements on systems without the need for a bit clock or pattern trigger thereby providing a simple and easy to use setup.

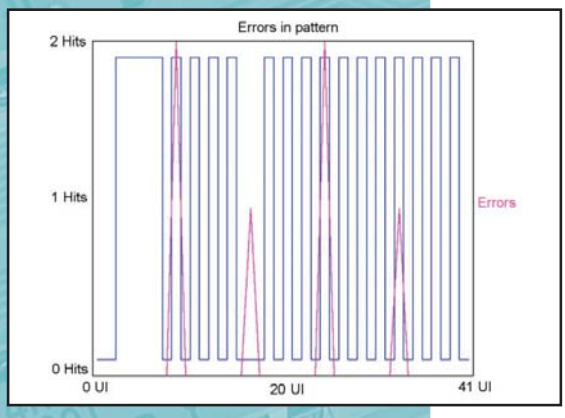
The Pattern Marker option enables the user to simply input a data stream with a repeating pattern into an SIA solution and obtain quantitative information on DJ, RJ, PJ, DCD&ISI and their contribution to Total Jitter. The Pattern Marker option produces a pattern marker from a unique portion of the pattern or by counting a user specified number of data edges. The pattern marker option decreases the measurement time compared to using a pattern generator pattern marker or pattern trigger because it generates a marker for every pattern repeat. For example, a typical data analysis on a PRBS 2^{15}-1 pattern at 1.5 Gb/s will take ~2 minutes with the pattern marker option but over 20 minutes using a pattern marker from a pattern generator with a marker density of 1/16. Additionally, the pattern marker card, along with GigaView(tm) software, automatically locates the marker in a low transition density region of the pattern eliminating the need to use delay lines to place the pattern marker in an optimal location ensuring reliable and repeatable results.

The Pattern Marker option also has the capability to detect bit errors in the pattern. The user can view the errors and their location in the pattern as illustrated in Figures 9 and 10. The ability to detect bit errors provides additional information about low probability errors, pattern dependent errors and is useful in jitter tolerance measurements to determine the BER. Bit error counting can be performed at distinct frequencies in pattern match mode.

Typical applications include jitter measurements on Host Bus Adapters, Host Channel Adapters, Target Channel Adapters, GBICs, IC's as well as other systems and components. Standard SIA 3600D and 3300D configurations consist of one Pattern Marker card and 2, 4 or 5 channel cards. Other configurations are available upon request.

PM50 Performance Specifications

Data rates for pattern match mode and bit error counting	1.0625, 1.25, 1.5, 2.125, 2.5, 3.0, 3.125, 3.1875 Gb/s ± 0.1%
Data rate range for edge count mode	Continuous up to 5.0 Gb/s
DCD&ISI Noise floor	≤1% added to individual channel card specification
Pattern requirements for or pattern match mode	Pattern must be 10, 20, 40 bits divisible by 40. 40-bit pattern match word must contain a K28.5 character
Pattern requirements for Bit Error counter	>40 bits
Pattern requirements for edge count mode	None



Plot 9

Pattern Marker Summary

Pattern Marker	Mode	Standard
PM1	Pattern Match	2X FC 2.125 Gb/s
Pattern File	**Total Delay**	**Edge Count**
idle.ptn	0s	16
20-bit Errors	**Total Compares**	**BER**
6	29.267258e9	2.050072e-010

Pattern Repeat	Frame Number	20-bit Data In Error	
596859123	0	0011111060	1010100010
615776191	0	0011111060	1010100010
634502766	0	0011111010	101010i010
652095529	1	1010101010	1060101010
669976830	1	1010601010	1010101010
685542942	1	1010601010	1010101010

Bir Error Count Table

Plot 10

Plot 10 shows the pattern and the number of errors for each bit in the pattern. In this example, there are six bit errors at four different bits in the pattern.

The table in Plot 10 shows the summary of the Bit Error Count information. This table shows the number of bit errors, BER, pattern repeat of the error, 20 bit frame in the pattern where the error occurred and the specific bit that was in error (indicated by a ^ above the number).

Clock Recovery

Continuous Rate 30 Mb/s to 3.0 Gb/s

Applicable Models: **3600D, 3300D**

The SIA solutions, with the addition of the clock recovery option, enable signal integrity compliance and diagnostics measurements when access to a bit clock is not available. The clock recovery option removes the need for awkward setups for obtaining accurate and repeatable compliant signal integrity measurements — simply plug in your test signal to make eye diagram and jitter measurements on any type of data signal, random or repeating.

Specifications

Clock recovery data rate	30 Mb/s to 3 Gb/s
Clock recovery PLL bandwidth	Databaud/1244 Typical Clock jitter*
Databaud < 500 Mb/s	< 5.0ps RMS
Databaud > 500Mb/s	< 3.0ps RMS
Insertion Loss Through Path	8 dB Typical
Operating Input Signal Level	
Single Ended:	0.250 to 2.5 Volts(pk-pk)
Differential:	0.125 to 1.25 Volts(pk-pk)

*Measured using PRBS $2^{\wedge 23}$-1 test pattern.

Setup

The data from the DUT is sent into the Clock recovery Data In. The supplied Hard-line SMA's are used to connect from the Clock Recovery Data Out to the IN1 (Channel 1 input). The recovered clock is used internally for all signal integrity measurements.

Applications

Fibre Channel (1x, 2x, 3x), SAS & SATA (1.5 & 3.0), Gigabit Ethernet, PCI Express, Infiniband, SONET OC-3,12,48, XAUI, 10GFC, Serial RapidIO, DVI, 1394b (800Mb/s & 1.6Gb/s), Fast Ethernet, HDMI, Custom (30 to 3000 Mb/s).

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